DEVELOPMENT OF HIGH EFFICIENCY MONOCRYSTALLINE SI SOLAR CELLS THROUGH IMPROVED OPTICAL AND ELECTRICAL CONFINEMENT

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DEVELOPMENT OF HIGH EFFICIENCY MONOCRYSTALLINE SI SOLAR CELLS THROUGH IMPROVED OPTICAL AND ELECTRICAL CONFINEMENT

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This work is dedicated to

my mother, Ms. Mieko Meemongkolkiat for her support and patience

my father, Mr. Pipop Meemongkolkiat for his support and patience

my sisters, Ms. Malika and Ms. Darunee Meemongkolkiat for their support

my friends, for their support

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LIST OF SYMBOLS AND ABBREVIATIONS

PV	Photovoltaics
BSF	Back surface field
Cz	Czochralski
LID	Light-induced degradation
PECVD	Plasma-enhanced chemical vapor deposition
SRH	Shockley-Read-Hall
τ	Recombination lifetime or lifetime
τ_{n0}	Characteristic electron lifetime
τ_{p0}	Characteristic hole lifetime
Δn	Injection level
σ	Capture cross-section
S or **SRV**	Surface recombination velocity
S_{n0}	Characteristic electron surface recombination velocity
S_{p0}	Characteristic hole surface recombination velocity
J_0	Reverse saturation current density
CVD	Chemical vapor deposition
V_{oc}	Open-circuit voltage
FGA	Forming gas anneal
PERC	Passivated emitter and rear cell
PERL	Passivated emitter, rear locally diffused
LBSF	local back surface field

FZ	Float zone
RTP	Rapid thermal processing
J_{sc}	Short-circuit current density
IQE	Internal quantum efficiency
SEM	Scanning electron microscope
NREL	National renewable energy laboratory
BSRV	Back surface recombination velocity
LBIC	Light beam induced current
ECV	Electrochemical capacitance-voltage
FF	Fill factor
Q_{FB}	Flat band equivalent charge density
FSRV	Front surface recombination velocity
R_s	Series resistance
R_{sh}	Shunt resistance
n_2	2^{nd} diode ideality factor
J_{01}	1^{st} diode reverse saturation current density
J_{02}	2^{nd} diode reverse saturation current density

SUMMARY

Solar cells are one of the most promising candidates for sustainable and environmentally friendly energy source because they convert sunlight directly into electricity with zero emission and no undesirable impact on the environment. However, photovoltaics (PV) or solar electricity currently contributes to a very small fraction of the total word energy production (<0.1%) because energy produced by PV is still about two to four times more expensive than the traditional energy sources. To compete with fossil fuels, price of a PV module must come down to around $1.00-1.50 per watt as opposed to around $4 per watt today. This will result in an installed PV system cost of about $3.50 per watt, which can produce electricity at about 8 cents/kWh to compete with fossil fuels.

Si solar cells account for ~90% of the PV modules being produced today, and the Si material alone accounts for ~50% of the cost of a Si PV module. The most obvious way to reduce its cost is to minimize the use of Si by reducing the thickness of the Si cells. Use of thinner Si substrates presents two major challenges: (1) process yield: the fabrication process should be simple and should not introduce high stress to prevent breakage and warping of the wafers and (2) cell performance: thinner substrates require high-quality surface passivation and optical confinement to enhance light absorption and carrier collection.

The objective of this thesis is to understand and improve optical and electrical confinement to achieve cost-effective high-efficiency Si solar cells on thin Si substrates. The optical confinement in Si solar cells is generally achieved by texturing of the front surface (light-incident surface) in conjunction with a formation of a high internal

reflective layer on the back surface. Electrical confinement is achieved through the use of a Si material with a high minority-carrier lifetime coupled with high-quality passivation of both surfaces.

In this thesis, a B-doped monocrystalline Czochralski (Cz) Si material with (100) orientation was investigated because it can be easily and effectively textured by an alkaline etch to enhance the optical confinement. However, B-doped Cz Si is known to suffer from lifetime degradation because of the formation of a B-O complex under illumination. The substitution of B by Ga as a p-type dopant can virtually eliminate the light-induced degradation (LID) effect because B is a source of the formation of the LID defects. Ga is currently not widely used in Si solar cells because of a significant resistivity variation along the length of a Ga-doped Cz Si ingot, relative to a B-doped ingot, because of a much lower segregation coefficient of Ga in Si. In the first task of this thesis, an attempt is made to evaluate quantitatively the benefits of Ga doping on the bulk lifetime, cell performance and the LID, and to investigate the undesirable effect, if any, of the resistivity variation on the cell performance variation along the length of the Ga-doped ingot. In this study, a commercially grown Ga-doped Cz Si ingot (925-mm long) is examined side by side with its B-doped Cz Si counterpart (950-mm long). It is important to note that, to maintain good control, both ingots were grown using the exact same facility at the Shell Solar Industry. Even though both the ingots were targeted to have a nominal resistivity of 1 ohm-cm, but as expected, a much wider resistivity variation was observed in the Ga-doped Cz Si ingot (0.57-2.54 ohm-cm) compared to the B-doped Cz Si ingot (0.87-1.22 ohm-cm). The variation in the post-diffusion bulk minority-carrier lifetime before LID was also found to be much more in the Ga-doped Cz Si ingot (100-

1000 μs) because of the resistivity variation; the B-doped Cz Si ingot from the seed to the tail end showed a lifetime in the range of 300-400 μs, except at the seed end where the lifetime was somewhat lower. Despite the large resistivity and lifetime variations in the Ga-doped Cz Si ingot, the variation in the absolute efficiency of the screen-printed Al-back surface field (BSF) solar cells was found to be less than 0.5% absolute, 16.8-17.3%, over the entire length of the ingot. Additionally, the Ga-doped Cz Si cells showed no LID at all after > 24 hours 1-sun illumination. On the other hand, the bulk lifetime of the B-doped samples decreased from 300-400 μs to ~20 μs after the LID, resulting in significant degradation in the cell efficiency from 16.7% to 15.6%. As a result, the 0.5-2.5 ohm-cm Ga-doped Cz Si cells gave ~1.5% higher average stabilized efficiency compared to the 1 ohm-cm B-doped Cz Si cells. These results demonstrate great potential of Ga-doped Cz wafers for achieving high-efficiency Si solar cells with no LID.

The second major task in this thesis involves back-surface passivation to enhance the electrical and optical confinement in p-type Si solar cells so that thin Si wafers can be used without sacrificing the cell efficiency. In this task, the widely used screen-printed full-area Al-BSF passivation was investigated to quantitatively assess its potential and limitations for achieving the desired electrical confinement for high-efficiency thin Si cells. The quality of the screen-printed Al-BSF was investigated as a function of: (1) surface texturing, (2) oxygen content in the materials, and (3) the thickness of printed Al in conjunction with the peak alloying temperature. Three important and novel findings were made. First, it was found that textured surfaces required a higher ramp-up rate to obtain a uniform BSF layer compared to planar surfaces. For Al printed thickness of 25 μm, a ramp-up rate of 50°C/s was sufficient to get a uniform BSF layer on planar back

surfaces, but this threshold value increased to 100°C/s for textured back surfaces. This is because textured surfaces are more difficult to alloy uniformly compared to planar surfaces. This finding is important because most cell manufacturers texture both surfaces of the wafer for process simplicity. Second, this study revealed that the screen-printed Al-BSF cells fabricated on regular Cz Si with high O_i content repeatedly gave higher back surface recombination velocity (BSRV) values compared to those fabricated on FZ Si. Magnetic Cz (MCz) cells with low O_i content did not exhibit this enhanced recombination. The observed effect of higher BSRV is conjectured to be a result of the O-precipitation induced defects residing at the p-p^+ interface. The important and third finding about the conventional screen-printed Al-BSF was that there exists a critical alloying temperature for a given Al-thickness, above which the Al-BSF becomes non-uniform and solar cell performance starts to degrade. This critical temperature is lower for thicker Al layers, which puts a limit on the maximum thickness of the Al-BSF that can be achieved. It was found that the non-uniformity in the Al-BSF layer is a result of the agglomeration of the Al-Si melt at higher temperatures. It was demonstrated that this non-uniformity in the Al-BSF layer, in combination with the band gap narrowing effect, because of greater than expected doping, has a detrimental effect on solar cell performance. It was then established that a proper combination of a BSF thickness and a peak doping concentration is crucial to obtain the best passivation quality from the screen-printed Al-BSF. Finally, the lowest BSRV value achieved in this work with the conventional screen-printed Al-BSF was 300 cm/s on 1.3 ohm-cm FZ Si. This was achieved through the use of a relatively thick Al-thickness of ~60 μm and a relatively low peak firing temperature of 750°C.

The previous task revealed why, in practice, it is difficult to reach the full potential of the screen-printed Al-BSF. A higher quality BSF required very thick Al, which would warp thinner substrates during the Al-BSF formation. In addition, the low-to-moderate reflectance (~60%) inherently associated with the Al-Si alloyed back surface will hurt the light trapping and the performance of cells made on thinner substrates. Therefore, in the following tasks, a dielectric/metal back contact system is investigated and developed using low-cost manufacturable technologies.

Prior to the process development for fabricating dielectric back-passivated p-type Si solar cells, device simulations were performed to understand the requirements and to develop a cell design where dielectric back passivation can be applied using a low-cost process. Because of the multi-dimensional nature of the dielectric back-passivated cell with local back contacts, a multi-dimensional semiconductor device simulation program DESSIS^{TM} was used in this study. The first part of the simulation task involved establishing the size and the spacing of the openings through the dielectric to achieve the best compromise between the resistance and the contact-induced recombination. The optimum spacing of the openings was found to be a function of several key cell parameters such as the size and the geometry of the opening, the base resistivity, and the contact recombination velocity. The key finding from these simulations was that, besides the necessity of having a local BSF (LBSF) at the openings to achieve high cell performance, the presence or absence of a lateral BSF region around the openings plays an important role in dictating cell performance as well as the optimum spacing. This is because, in the absence of the lateral BSF, the high recombination at the edge of the back contact is not suppressed and can greatly enhance the overall recombination at the back

contact. For example, in the case of 150-μm square openings on 2.0 ohm-cm substrates, the optimum cell efficiency reduced by 0.5% absolute, from 20.4% to 19.9%, in the absence of the lateral BSF, while the optimum spacing increased from 500 μm to 800 μm.

In the second part of the simulation task, 2-D simulations were performed to investigate the effect of charge in the dielectric layer on the performance of dielectric back-passivated p-type Si solar cells. A new simulation methodology was developed and incorporated into the Dessis program to simulate the effect of the inversion layer shunting as a function of the positive charge density in the back dielectric layer. It was established that for p-type Si cells with a severe parasitic shunt path between the inversion layer and the back contact, the dielectric positive charge density should be kept at around 2.5×10^{11}, 1.5×10^{11}, 1.0×10^{11}, and 4.0×10^{10} cm^{-2} for the base resistivity of 0.5, 1.0, 2.0, and 6.0 ohm-cm, respectively. It was also found that, for p-type cells, negative charge in the back dielectric layer is more desirable and higher amount of negative charge leads to better cell performance.

From the numerous simulation results, two key requirements for achieving high-efficiency dielectric back-passivated p-type Si solar cells were established: (1) a formation of a high quality LBSF, preferably with a lateral BSF and (2) use of a dielectric layer that not only provides a high-quality passivation, but also contains either a moderate positive charge density or a high negative charge density. This led to the fourth task in this thesis, which involved development of (1) a low-cost metallization technique that forms a high quality LBSF and (2) a dielectric layer with high-quality surface passivation and a desirable amount of the charge density. It should be noted that the

above two developments are interdependent because the desired characteristics of the dielectric layer should be maintained after the application of the metallization process. Often, screen-printed contact firing alters or degraded the passivation quality of the dielectric layer. To develop dielectric back-passivated cells with a LBSF, low-frequency plasma-enhanced chemical vapor deposition (PECVD) SiN_x (LF-SiN_x) was chosen as one of the key layers for the back dielectric because (1) a deposition of LF-SiN_x by the PECVD method is a high-throughput process and (2) LF-SiN_x can also serve as a masking layer against metal impurities. The technology to achieve local contacts, a LBSF, and a back surface reflector involves a formation of local openings through a dielectric layer prior to full-area Al screen-printing and rapid firing. In this research, a novel Al paste was developed that was able to (1) form a uniform and thick (>10 μm) LBSF layer through the openings in the dielectric layer, (2) maintain the passivation quality of the dielectric layer without punching through, and (3) form a good back reflector with internal back reflection of > 85%. Modifications to the Al paste involved removal of the glass-frit and an addition of 7-12 % Si. The use of the modified Al paste resulted in ~1% absolute higher efficiency compared to a conventional Al paste on the dielectric back-passivated cell (16.0% versus 15.0%). However, the efficiency of the dielectric back-passivated cell with this modified Al paste was still lower than that of the conventional full-area screen-printed Al-BSF cell by ~0.5% absolute (16.0% versus 16.5%). The inferior performance is attributed to the high positive charge density (> 1×10^{12} cm^{-2}) in the dielectric layer used in these experiments. This led to the development of novel spin-on dielectric layers with appropriate charge and characteristics, described below.

To develop novel dielectric layers for back surface passivation of p-type Si solar cells that can withstand contact firing and have appropriate charge, new SiO_2-based spin-on dielectric layers and several other conventional dielectric layers were investigated for their charge, interface property, and passivation quality. The two new spin-on dielectric layers were found to be effective: spin-on SiO_2 (2,600 Å) and spin-on Al-doped SiO_2 (1,300 Å). Conventional dielectric layers included in this study were thin thermally grown SiO_2 (80-100 Å), LF-SiN_x (index ~ 2.0), and stacked thin thermally grown SiO_2 (80-100 Å)/LF-SiN_x. The procedure to form the spin-on dielectric layers in this work involved: (1) spinning of a sol-gel precursor on a Si substrate, (2) drying at 200°C for 15 minutes, and (3) curing in O_2 ambient for 10 minutes followed by a N_2 anneal at 875°C for 10 minutes in a conventional tube furnace. Thin thermally grown SiO_2 in this work was formed using the same annealing recipe mentioned above.

Detailed characterization and analysis of the dielectric layers revealed that the new Al-doped spin-on SiO_2 exhibited a high negative charge density and high-quality surface passivation on p-type Si wafers immediately after it was formed. Unfortunately, the layer suffered from long-term instability that caused the negative charge density to reduce with time, which resulted in a loss of the passivation quality. On the other hand, the thick spin-on SiO_2 was found to be very similar to the thin thermal-SiO_2 in terms of the positive charge density ($<2\times10^{11}$ cm^{-2}). Unfortunately, they both required a hydrogenation step to achieve high-quality surface passivation, which degraded during rapid contact firing. This prevented their direct application to screen-printed solar cells. Next, it was found that the LF-SiN_x and the stacked thin thermal-SiO_2/LF-SiN_x provided high-quality surface passivation and high thermal stability against subsequent rapid firing, but they contained

a high positive charge density (>1×10^{12} cm^{-2}) resulting in an inversion layer induced shunting and lower cell performance.

After the above dielectric layers failed to provide the desirable characteristics, the two spin-on dielectric layers were capped with the LF-SiN_x for further investigation. Capping the spin-on Al-doped SiO_2 with the LF-SiN_x resulted in significant degradation in the passivation quality, which can be attributed to the reduction of the positive influence of the negative charge density by the presence of the high positive charge density in the LF-SiN_x film. However, the spin-on SiO_2 capped with the LF-SiN_x resulted in a dielectric system that exhibited an excellent surface passivation quality, high thermal stability subsequent to firing (an estimated surface recombination velocity of 20-25 cm/s on a 2.5 ohm-cm p-type substrate both before and after firing), and a desirable positive charge density (<2.5×10^{11} cm^{-2}). Consequently, the stacked spin-on SiO_2/LF-SiN_x showed the highest potential for use as a back surface passivation layer of p-type Si solar cells, and was chosen for use in the final device fabrication in this thesis.

In the fifth and final task of this thesis, screen-printed dielectric back-passivated p-type Si solar cells were fabricated using the metallization scheme involving Al-Si paste and the spin-on SiO_2/LF-SiN_x dielectric layer developed in the previous task. Via's were opened through the dielectric using a screen-printed etching paste, prior to applying the Al-Si paste on the rear and firing. The 4-cm^2 cells were fabricated on 300-μm thick FZ Si substrates. High screen-printed cell efficiency of ~19% was achieved with a BSRV value of ≤ 125 cm/s and internal back surface reflectance of 85-95 %. The dielectric back-passivated cells produced about 0.3-0.8% absolute efficiency higher than that of the

conventional Al-BSF back-passivated cells, which had a BSRV of ~ 300 cm/s, back surface reflectance of ~68%, and a similar front structure.

The dielectric back-passivated high-efficiency cell developed in this thesis were simulated with great accuracy through a combination of detailed characterizations and modeling using a 1-D simulation program (PC1D) as well as a 2-D simulation program (Dessis). The analysis revealed that there are three areas that can be improved for achieving even higher efficiencies: (1) reduction of the leakage current, (2) reduction of the series resistance, and (3) elimination of the parasitic shunt path between the rear inversion layer and the back contact. These improvements can lead to >20% efficient screen-printed cells on 100-μm thick Si substrates, which will bring Si PV close to grid parity.

CHAPTER 1

INTRODUCTION AND RESEARCH OBJECTIVES

1.1 Statement of the Problem

The emission of CO_2 and greenhouse gases has increased rapidly since the start of the industrial evolution in 1750 (Figure 1.1) [1]. This is the result of the extensive use of fossil fuels to satisfy the rapid increase in the global energy demand (Figure 1.2) [2]. Because of the rapid depletion of fossil fuels and their undesirable impact on the environment, there is an urgent need to find clean and sustainable sources for energy. Combustion of fossil fuels generates greenhouse gases, such as CO_2, which cause global warming and climate change.

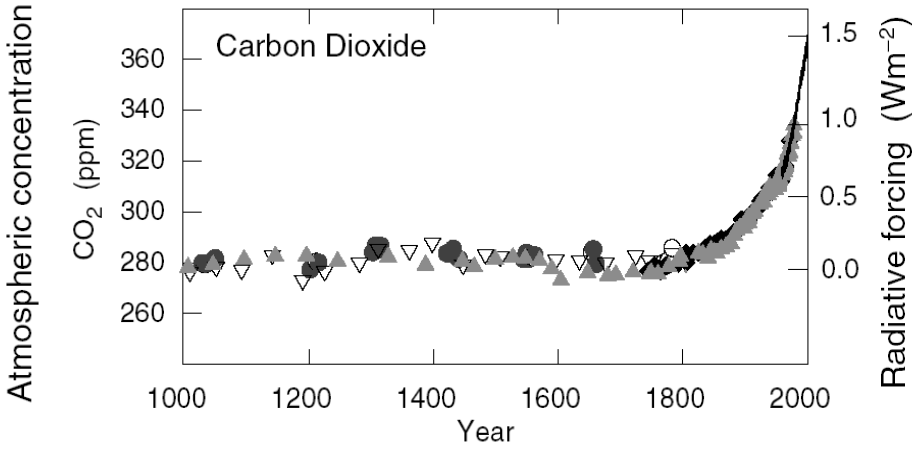


Figure 1.1 Atmospheric concentration of CO_2 in the past 1000 years [1].

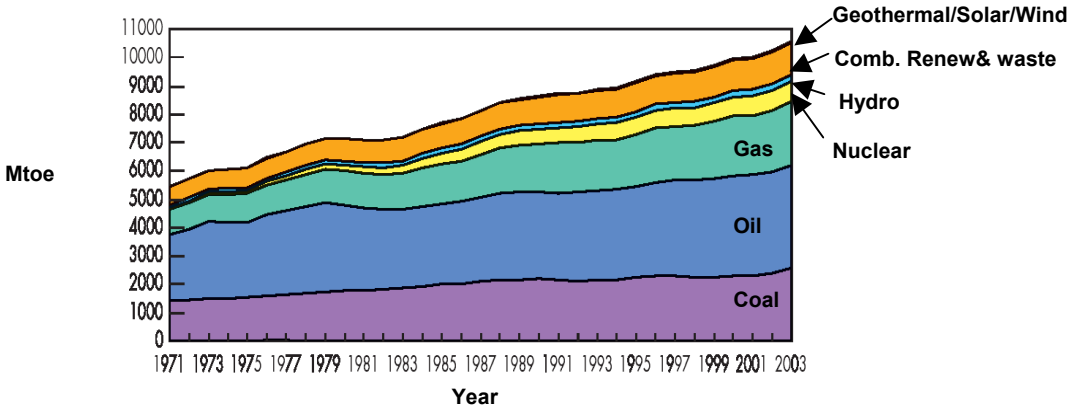


Figure 1.2 Evolution of the world total primary energy supply during 1971-2003 [2].

Rapid climate change becomes a threat to all living beings, as the ecosystem cannot accommodate for such rapid changes. Examples of threats to human beings include water resources, agriculture (food security), human settlements, etc. In response to this challenge, number of technologies are being developed that could substantially reduce the CO_2 emission. Some examples include the use of fossil-fuel with CO_2 capture and storage, nuclear fission, fusion energy, hydrogen, biofuels, fuel cells, solar, and efficient energy end use [3].

Among the various alternatives, solar cells offer a unique opportunity to solve the energy and environmental problems simultaneously because sunlight, which is free and unlimited, is the fuel for solar cells, and solar cells can convert it into electrical energy with zero emission and pollution. A typical energy payback time of two to five years compared to an expected lifetime of 20-30 years for a photovoltaic (PV) system also suggests a benefit for the environment. However, solar cells currently contribute to a very small fraction of the total primary energy supply of the world (Figure 1.3). This is because the price of energy produced by solar cells is still two to four times more

expensive than fossil fuels (Figure 1.4). To compete with fossil fuels, the overall PV cost must come down to approximately 6-8 ¢/kWh for base load applications and about 15 ¢/kWh for peak load applications. This corresponds to a module cost of about $1.0-$1.5/Watt. Unfortunately, the present cost of PV modules is around $4/Watt.

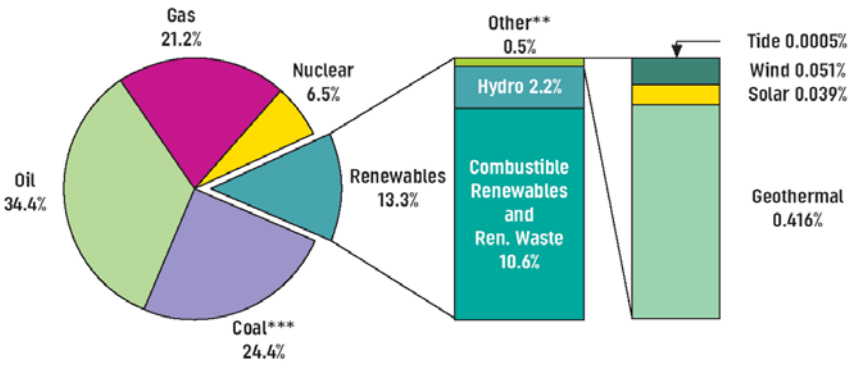


Figure 1.3 Fuel shares of the world total primary energy supply in 2003 [2].

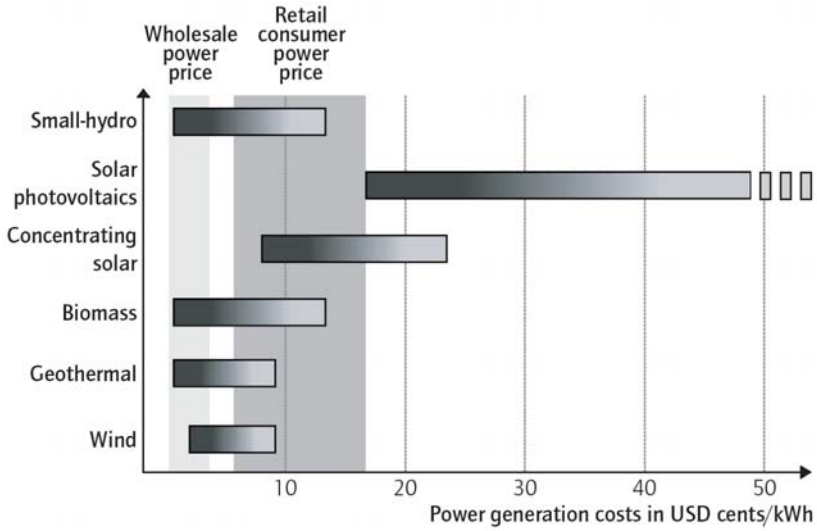


Figure 1.4 Cost competitiveness of selected renewable energies [4].

One of the main strategies to promote applications of PV is to improve the efficiency of solar cells while bringing the fabrication cost down. This is challenging because improvement in solar cell efficiency often requires a more complicated process, which leads to a higher production cost.

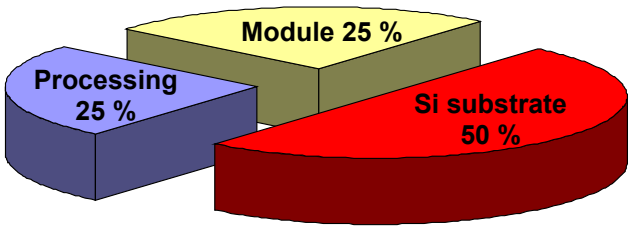


Figure 1.5 Cost breakdown of a Si solar cell module (calculated for mono- or multi-crystalline Si solar cells based on the data provided in [5].)

Currently, Si solar cells account for ~90% of the PV for terrestrial use [6] and Si alone accounts for ~50% of the cost of a Si PV module (see Figure 1.5). Therefore, the best way to reduce the cost of a Si PV module is to minimize the use of Si by reducing its thickness without compromising the cell efficiency. However, use of thinner substrates requires two main considerations: (1) maintaining the process yield: the fabrication process should be simple and should not introduce high stress on the substrate and (2) maintaining cell performance: thinner substrates require high-quality surface passivation and texturing for superior electrical and optical confinement of carriers.

Currently, the dominant technology for p-type Si solar cells involves screen-printing based metallization (Figure 1.6). A p-type Si substrate is first subjected to a P-diffusion to obtain a p-n junction. A nitride layer is then deposited on the front for antireflection coating and front surface passivation. Subsequently, Al paste is screen-printed for the entire backside followed by Ag gridline printing on the front. The sample is then

subjected to spike firing with a peak temperature of 700-850°C for the electrical contact formation. Use of Al on the backside also provides an Al-doped Si (p^+-Si) back surface field (BSF) during the contact formation, which serves as a back surface passivation layer. Unfortunately, the Al-BSF may not be adequate for thinner substrates because its formation introduces high stress, which can warp thin wafers. In addition, the Al-BSF provides only low-to-moderate quality surface passivation and it exhibits low internal surface reflection, which are not sufficient for excellent electrical and optical confinement, respectively.

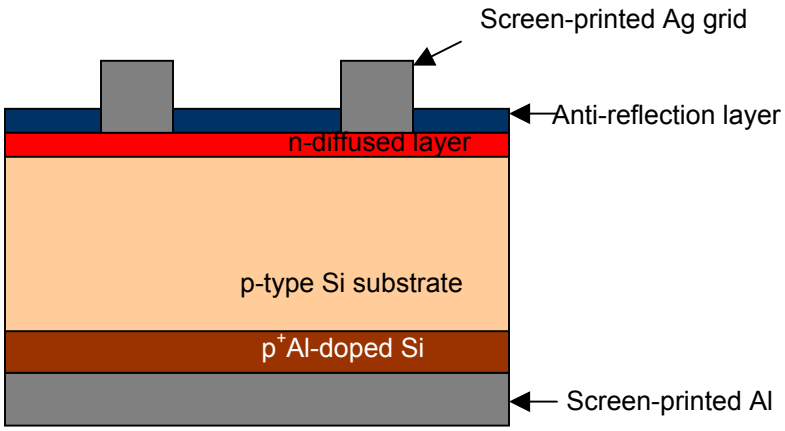


Figure 1.6 Common screen-printed p-type Si solar cell structure.

The objective of the research in this thesis is to understand and improve optical and electrical confinement to achieve cost-effective high-efficiency thin Si solar cells. Optical confinement in Si solar cells is generally achieved by texturing of the front surface (light-incident surface) in conjunction with a formation of a high internal reflective layer on the back surface. Electrical confinement is obtained through the use of a Si material with a high minority-carrier lifetime coupled with high-quality passivation on both surfaces.

In this research, B-doped monocrystalline Czochralski (Cz) Si is used because it can be easily and effectively textured by an alkaline etch to enhance the optical confinement. However, B-doped Cz Si is known to suffer from lifetime degradation because of the formation of a B-O complex under illumination. Therefore, Ga is investigated as a substitute for B in this research to maintain a high lifetime, which is necessary for high-efficiency cells. Another major area of investigation involves back surface passivation to enhance electrical and optical confinement. It is shown that the widely used screen-printed Al-BSF for back surface passivation is not sufficient for providing very high-efficiency cells on thin Si substrates. Therefore, a dielectric/metal back contact system is investigated and developed using low-cost manufacturable technologies.

1.2 Specific Research Objectives

The overall goal of this thesis is to develop high-efficiency solar cells on mono-crystalline Si by enhancing electrical and optical confinement of photogenerated carriers. This is accomplished through a combination of cell design, low-cost technology development, and a fundamental understanding of the loss mechanism associated with bulk and surface qualities. The research in this thesis is divided into five tasks. Task 1 is to investigate the merit of using Ga-doping in crucible-grown Cz Si to achieve a high bulk lifetime and to minimize light-induced degradation (LID) in Cz Si cells. In Task 2, a fundamental understanding of the widely used screen-printed Al-BSF is developed to assess its back surface passivation quality. In Task 3, 2- and 3-D simulations are performed using the simulation program DESSIS^{TM} to improve the fundamental understanding and establish requirements and design of high-efficiency dielectric back-passivated Si solar cells. Based on the simulation results, a cell structure is proposed

along with a low-cost process sequence to fabricate such a structure. Task 4 involves a combination of technology development and characterizations to achieve the desired characteristic of the back dielectric as well as the back contact. Finally, in Task 5, complete solar cells are fabricated with dielectric back passivation with local contacts and local BSF (LBSF). These cells are characterized and analyzed in detail to enhance the theoretical and experimental understanding of low-cost dielectric back passivation for Si solar cells.

1.2.1 Task 1: Investigation of Ga-Doped Cz Si Materials for High-Efficiency Si Solar Cells

The main drawback of using conventional B-doped Cz Si is the LID, which can result in appreciable degradation in cell performance after prolonged light exposure. The substitution of B by Ga as a p-type dopant in the base can virtually eliminate this effect because B is involved in the formation of the light-induced defects. In addition, there is a possibility that a Ga-doped Cz material might give a higher starting lifetime because Ga is less prone to forming lifetime-limiting defects during crystal growth. However, Ga is not widely used in Si solar cells today because of a significant resistivity variation along the length of a Ga-doped Cz Si ingot relative to a B-doped ingot. This is because of the much lower segregation coefficient of Ga in Si. Nevertheless, this could be solved by continuous melt replenishment or it may not introduce efficiency variation along the ingot. This is because loss in voltage can be offset by a gain in current as the resistivity increases. This provided the motivation to investigate the merit of using a Ga dopant. In Task 1, an attempt is made to evaluate the benefits of Ga doping on the bulk lifetime and the LID and compare it with the negatives, if any, of the resistivity variation, which may lead to a performance variation along the length of the ingot. In this task, first, the quality

of a commercially grown Ga-doped Cz Si ingot is examined side by side with its B-doped Cz counterpart. This is done by examining the bulk lifetime (before and after the light exposure) of samples taken from different locations along the two ingots. It is important to note that to maintain good control, both ingots were grown using the exact same facility at the Shell Solar Industry. To examine the impact of the Ga doping and the resistivity variation on the LID and solar cell performance, complete screen-printed solar cells with Al-BSF were fabricated and analyzed.

1.2.2 Task 2: Investigation of the Potential and the Limitations of the Conventional Full-Area Al-BSF for Achieving High-Efficiency Si Solar Cells

The screen-printed Al-BSF is by far the most favorable technique in industry for back surface passivation of solar cells because of its simplicity, effectiveness, and cost. However, to realize higher efficiency cells on thinner substrates, which is the hope and the trend in the PV industry, a much higher back surface passivation quality may be required. Theoretically, the Al-BSF should have the potential to provide acceptably high-quality surface passivation. However, experimentally, this may not be the case. Therefore, the purpose of this task is to investigate quantitatively the potential and/or the limitations of the screen-printed Al-BSF for achieving the desired electrical confinement for thin Si cells. In this task, the quality of the Al-BSF is investigated with respect to the following factors: surface texturing, oxygen content in the materials, and the thickness of printed Al in conjunction with the peak alloying temperature.

1.2.3 Task 3: Design of Dielectric Back-Passivated Solar Cells through 2- and 3-D Device Modeling

It has been proven that a thermally grown SiO_2, a plasma-enhanced chemical vapor deposition (PECVD) SiN_x, or a combination of both provides excellent passivation of a

Si surface. However, the application of such dielectric systems for back surface passivation of Si solar cells fabricated with low-cost, high-throughput screen-printed contacts has never been demonstrated. The challenge lies in the development of a low-cost process to form a good electrical contact through these dielectric layers without degrading the passivation quality or to develop a new dielectric system that can withstand a screen-printing process. Therefore, the purpose of this task is to examine the requirements and to develop a cell design where the dielectric back passivation can be applied through a low-cost process. This involves establishing (1) the size and spacing of the contact windows through the dielectric layer to achieve the best compromise between resistance and contact-induced recombination and (2) the desired properties of the dielectric layer, focusing on the amount of charge in the dielectric layer.

Device simulations are first performed using the 2- and 3-D semiconductor simulation program Dessis to gain an understanding of the requirements to achieve a high-performance dielectric back-passivated solar cell. Subsequently, a solar cell structure is proposed along with a low-cost process sequence to fabricate it.

1.2.4 Task 4: Low-Cost Technology Development for Fabricating Dielectric Back-Passivated Solar Cells

This task involves process developments to achieve the cell structure and the requirements established in the previous task. This includes (1) the development of dielectric systems for excellent back surface passivation, (2) establishing a low-cost process for opening contact windows through the dielectric, and (3) making an ohmic contact and a LBSF through the windows while maintaining the passivation quality of the dielectric passivation.

1.2.5 Task 5: Fabrication and Analyses of Dielectric Back-Passivated Solar Cells

The final task involves integrating and implementing the processes developed in Task 4 to fabricate complete dielectric back-passivated solar cells with a LBSF on p-type Si substrates. A number of electrical and optical measurements are performed to characterize the dielectric back-passivated screen-printed cells. These cells are compared with the conventional full-area screen-printed Al-BSF cells to assess the efficiency of the back surface passivation. Finally, cell data are fed into a device model to compare the theoretical and experimental results for the dielectric back-passivated cells and to provide guidelines for further improvements in the important technology for next-generation solar cells.

CHAPTER 2

RECOMBINATION IN SI SOLAR CELLS

Electricity generation by Si solar cells relies on collection of photogenerated carriers at the p-n junction. Specifically, the photogenerated minority carriers at each side of the cell (electrons generated in the p-side and holes generated in the n-side) should travel to the junction, where they are swept to the other side by the electric field at the junction. Any loss or recombination of these excited carriers, before reaching the junction, contributes to a loss in cell performance. In a conventional p-type Si solar cell shown in Figure 2.1, recombination can occur in five regions:

(a) Front surface

(b) n-doped region or the emitter

(c) Depletion region of the p-n junction

(d) p-doped region or the base

(e) Back surface

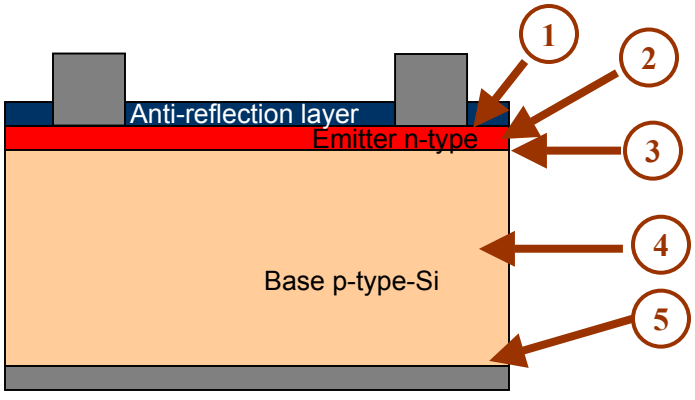


Figure 2.1 Five common recombination sites in a p-type Si solar cell.

The aim of this chapter is to provide a review of mechanisms responsible for the recombination activity in Si solar cells. First, the three fundamental recombination mechanisms in bulk semiconductors are discussed followed by the surface recombination. Subsequently, the theory of carrier transport in a semiconductor is covered since it plays an important role in dictating the net carrier recombination throughout the device.

2.1 Fundamental Recombination Mechanisms in a Semiconductor

There are three fundamental recombination mechanisms in a bulk semiconductor:

(a) Radiative or band-to-band recombination

(b) Auger recombination

(c) Recombination through defect or trap levels (often referred to as Shockley-Read-Hall recombination (SRH recombination))

Prior to going into the mathematical expressions of each of the three recombination mechanisms, it is instructive to introduce two main quantities that are commonly used to assess the volume recombination activity:

(a) Volume recombination rate, U_V ($cm^{-3}s^{-1}$)

: A recombination rate of carriers per unit volume per unit time

(b) Recombination lifetime, τ (s)

: An average time that excess carriers can survive before recombining

The lifetime can be expressed in terms of the volume recombination rate and the excess carrier concentration (Δn) as:

$$\tau \equiv \frac{\Delta n}{U} \ . \qquad (2.1)$$

Note that the use of the lifetime definition is valid only when there are excess carriers in the volume (non thermal equilibrium).

The excess carrier concentration or the injection level has a siginificant impact on the recombination behavior. Generally, the injection level is defined with respsect to the doping concentration as follows:

- Low-level injection (LLI) corresponds to the condition where the excess carrier concentration is smaller than the doping concentration by at least an order of magnitude

- High-level injection (HLI) corresponds to the condition where the excess carrier concentration is larger than the doping concentration by at least an order of magnitude

2.1.1 Radiative Recombination

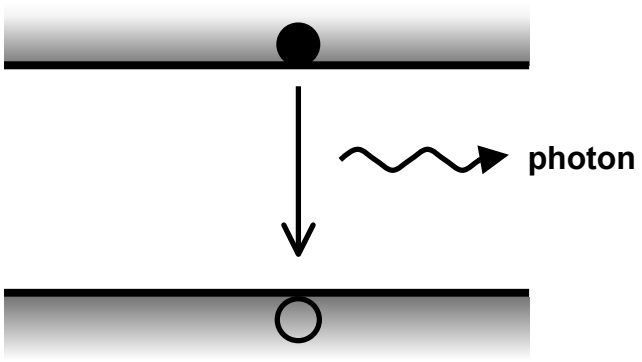


Figure 2.2 Schematic representation of radiative recombination.

Radiative recombination (also referred to as band-to-band recombination) corresponds to the recombination process where a free electron falls directly from the conduction band and recombines with a free hole in the valence band with all or most of the excess energy dissipated in the form of a photon (see also Figure 2.2). The radiative volume recombination rate, U_{BB}, is simply proportional to the electron concentration in

the conduction band (the free-electron concentration) and the hole concentration in the valence band (the free-hole concentration):

$$U_{BB} = Bnp \ , \tag{2.2}$$

where B is the coefficient of radiative recombination, n is the free-electron concentration and p is the free-hole concentration. From detailed balance calculation, the value of B for Si was calculated to be 2×10^{-15} cm^3s^{-1} [7, 8]. The experimental value, however, was found to be much higher: 9.5×10^{-15} cm^3s^{-1} [9].

At thermal equilibrium ($\Delta n=0$), U_{BB} is equivalent to the thermal generation rate, G_{th}; the expression for U_{BB} at thermal equilibrium is

$$U_{BB} = G_{th} = Bn_0p_0 = Bn_i^2 \ , \tag{2.3}$$

where n_0 and p_0 are the thermal equilibrium concentrations of free electrons and free holes and n_i is the intrinsic carrier concentration.

From Equation 2.1 and 2.2, the radiative recombination lifetime can readily be obtained as

$$\tau_{BB} = \frac{\Delta n}{B \cdot (n_0 + \Delta n) \cdot (p_0 + \Delta n)} \ . \tag{2.4}$$

Consequently, the expressions for the radiative recombination lifetime under low and high injection are as follows:

$$\tau_{BB,lli} = \frac{1}{B \cdot N_{doped}} \qquad \text{and} \qquad \tau_{BB,hli} = \frac{1}{B \cdot \Delta n} \ , \tag{2.5}$$

where N_{doped} is the donor (N_D) or the acceptor (N_A) concentration for n- or p-type semiconductors, respectively. Note that the radiative recombination lifetime stays

constant at low injection and decreases with injection in intermediate and high injection regimes.

The radiative recombination in an indirect band gap semiconductor such as Si is considered to be small compared to other types of recombination. This is because the process involves phonon as the fourth particle (apart from an electron, a hole, and a photon) to conserve the momentum (see Figure 2.3).

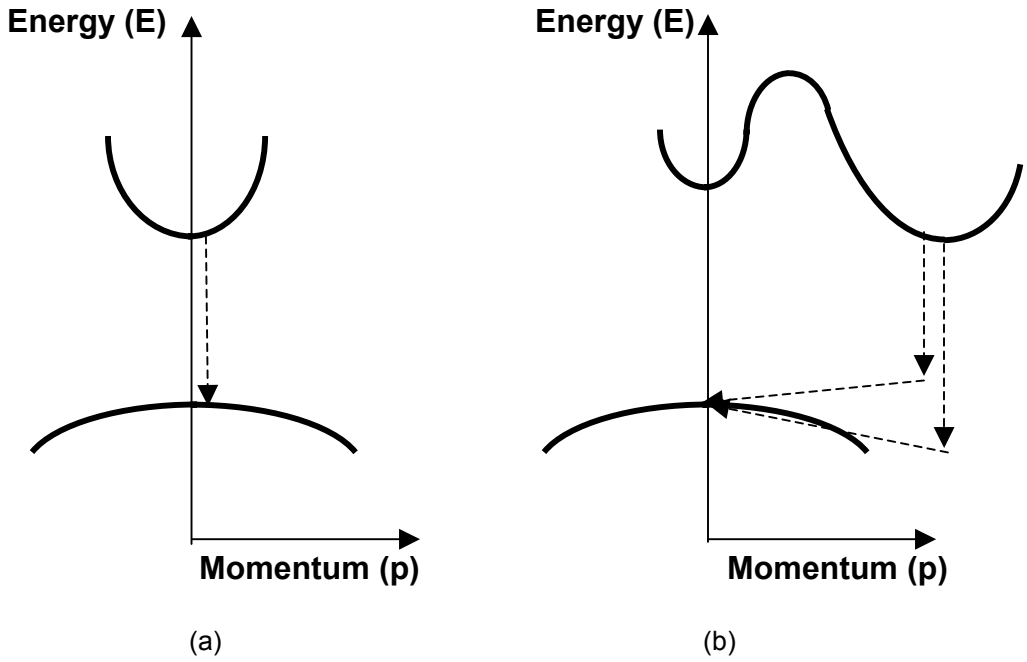


Figure 2.3 Schematic representation of radiative recombination for (a) direct band gap (e.g. GaAs) and (b) indirect band gap (e.g. Si).

2.1.2 Auger Recombination

Auger recombination is a three-particle interaction where an electron in the conduction band and a hole in the valence band recombine giving the excess energy to the third electron or hole (see Figure 2.4). eeh and ehh denote the cases where the excess

energy is transferred to an electron and a hole, respectively. The Auger recombination rate, U_{Auger}, is given by

$$U_{Auger} = U_{eeh} + U_{ehh} \text{ or} \tag{2.6}$$

$$U_{Auger} = C_n \cdot n^2 \cdot p + C_p \cdot n \cdot p^2 \ . \tag{2.7}$$

where C_n and C_p are the Auger coefficients for electrons and holes, respectively.

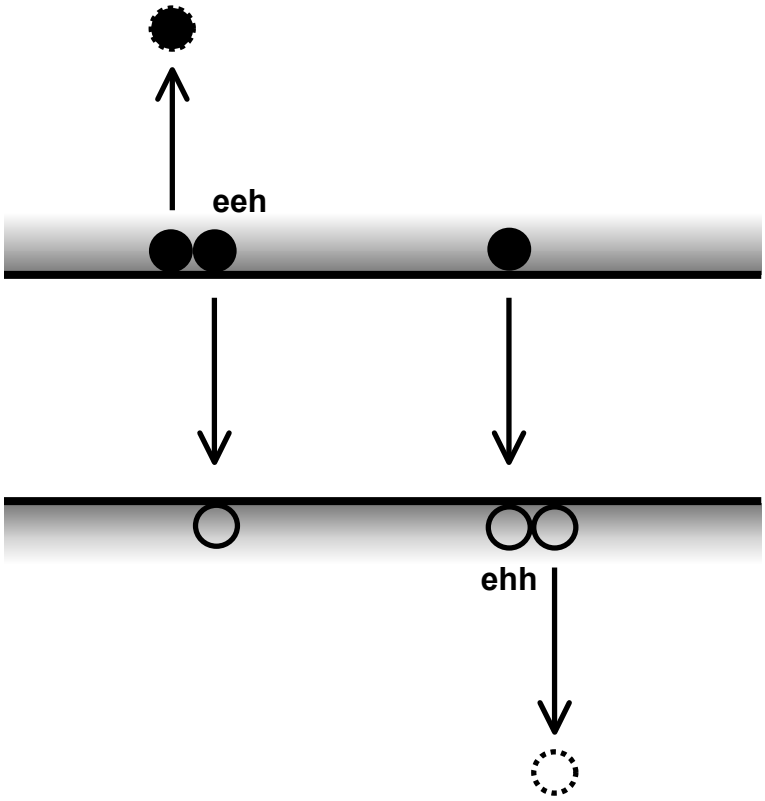


Figure 2.4 Schematic representation of Auger recombination.

Consequently, the expressions for the Auger recombination lifetime under low and high injection are as follows:

n-type Si $\tau_{Auger,lli} = \dfrac{1}{C_n \cdot N_D^2}$ and $\tau_{Auger,hli} = \dfrac{1}{(C_n + C_p) \cdot \Delta n^2}$ and (2.8)

p-type Si $\tau_{Auger,lli} = \frac{1}{C_p \cdot N_A^2}$ and $\tau_{Auger,hli} = \frac{1}{(C_n + C_p) \cdot \Delta n^2}$. (2.9)

The most commonly used values for the Auger coefficients were determined by Dziewior and Schmid (C_n=2.8×10^{-31} cm^{6}s^{-1} and C_p=0.99×10^{-31} cm^{6}s^{-1}) for Si with a doping concentration greater than 5×10^{18} cm^{-3} [10]. However, departures from these simple expressions have been experimentally observed and discussed in the literature. Detail on these departures along with one of the most recent parameterisation can be found in [11].

The Auger recombination lifetime is, to the first order, a quadratic function of the carrier concentration, as opposed to a linear function in the case of the radiative recombination lifetime. As a result, Auger recombination dominates the lifetime at high doping or at high injection.

2.1.3 SRH Recombination

Defects in semiconductors can create energy levels within in the band gap that can greatly enhance the recombination process. These trap levels form stepping stones whereby an electron falls from the conduction band to the defect level and then from the defect level to the valence band. This type of recombination normally dominates the net recombination rate in low quality materials with a high defect density.

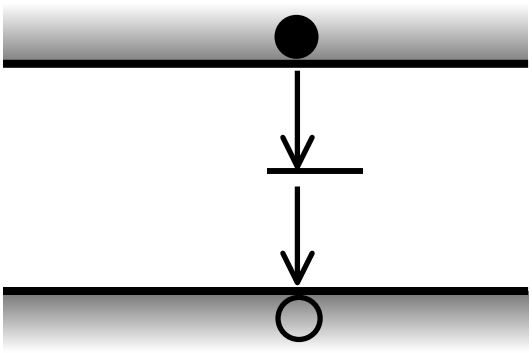


Figure 2.5 Schematic representation of recombination via a defect level.

The dynamic of the recombination process via trap levels inside the band gap was first derived by Shockley and Read and Hall (so-called SRH recombination theory) [12, 13]. Important assumptions made in the derivation of the SRH recombination rate are summarized in [14] and are listed below

(a) No radiative recombination or Auger recombination involves

(b) The semiconductor is non-degenerate

(c) The energy level of the defects does not change with their charging properties

(d) The relaxation time of the charge carriers caught by the defects is negligibly small compared to the average time between two emission processes

(e) Fermi-Dirac statistic applies

(f) The defects do not interact with each other (i.e., an electron cannot make a transition from a defect level to another.)

The SRH volume recombination rate, U_{SRH}, for single-energy level traps is then given by

$$U_{SRH} = \frac{np - n_i^2}{\tau_{p0}(n + n_1) + \tau_{n0}(p + p_1)} , \qquad (2.10)$$

where τ_{n0} and τ_{p0} are the characteristic electron and hole lifetimes, which are related to the thermal velocity of the charge carrier, υ_{th}, the defect concentration, N_t, and the capture cross-sections of electron and hole of the specific defect, σ_n and σ_p as

$$\tau_{n0} \equiv \frac{1}{\sigma_n \upsilon_{th} N_t} \text{ and } \quad \tau_{p0} \equiv \frac{1}{\sigma_p \upsilon_{th} N_t} \ . \tag{2.11}$$

n_1 and p_1 are defined as:

$$n_1 \equiv n_i \exp\left(\frac{E_t - E_i}{kT}\right) \text{ and } p_1 \equiv n_i \exp\left(\frac{E_i - E_t}{kT}\right) . \tag{2.12}$$

By definition, n_1 and p_1 are the free-electron and the free-hole concentrations in the case in which the Fermi level (E_F) lies at the trap energy level (E_t).

The SRH recombination lifetime can then be obtained as follows:

$$\tau_{SRH} = \frac{\tau_{p0}(n + n_1) + \tau_{n0}(p + p_1)}{n_0 + p_0 + \Delta n} \ . \tag{2.13}$$

Consequently, the expressions for the SRH recombination lifetime under low and high injection are as follows:

n-type Si $\quad \tau_{SRH,lli} = \tau_{p0} + \frac{\tau_{n0}(\Delta n + p_1)}{N_D}$ and $\quad \tau_{SRH,hli} = \tau_{n0} + \tau_{p0}$ and (2.14)

p-type Si $\quad \tau_{SRH,lli} = \tau_{n0} + \frac{\tau_{p0}(\Delta n + n_1)}{N_A}$ and $\quad \tau_{SRH,hli} = \tau_{n0} + \tau_{p0}$. (2.15)

For traps located at the middle of the band gap ($E_t \cong E_i$), both n_1 and p_1 become small and equal to n_i. Consequently, the SRH lifetime under low injection can further be simplified as:

n-type Si $\quad \tau_{SRH,lli} = \tau_{p0}$ for mid-gap traps and (2.16)

p-type Si $\quad \tau_{SRH,lli} = \tau_{n0}$ for mid-gap traps . (2.17)

As can be seen from Equation 2.14 through 2.17, with respect to the location of the traps in the band gap, the SRH lifetime becomes lowest when the traps lie at the middle of the band gap. Consequently, the mid-gap traps are considered to be the most harmful traps that can greatly enhance the overall recombination in the device.

In reality, all three recombination processes discussed above take place at the same time. The net volume recombination can be obtained simply by adding the three recombination rates as follows:

$$U_{net} = U_{BB} + U_{Auger} + U_{SRH} \ . \tag{2.18}$$

The net lifetime (τ_{net}) can, therefore, be obtained as:

$$\frac{1}{\tau_{net}} = \frac{1}{\tau_{BB}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} \ . \tag{2.19}$$

2.2 Surface Recombination

Surface recombination corresponds to a phenomenon where excited electrons in the conduction band recombine with holes in the valence band via defect levels at the surface, called surface states (Figure 2.6). These surface states are the result of the abrupt discontinuity of a crystalline phase at the surface, which forms unsatisfied dangling Si bonds. The recombination via these surface states can be explained through minor modification of the volume SRH recombination theory (Section 2.1.3). This is explained in detail below.

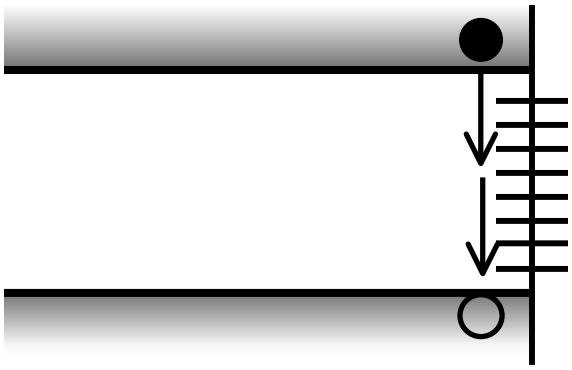


Figure 2.6 Schematic representation of recombination via surface states.

It is instructive to first introduce two main quantities that are used to assess the surface recombination activity :

(a) Surface recombination rate, U_s ($cm^{-2}s^{-1}$)

: A recombination rate of carriers per unit area per unit time

(b) Surface recombination velocity, S or SRV (cm/s)

: A velocity of the excited carrier flowing to a surface

The surface recombination velocity is related to the surface recombination rate by the following equation:

$$S \equiv \frac{U_s}{\Delta n} \ . \tag{2.20}$$

With minor modifications to the expression of the volume SRH recombination (Equation 2.10), the surface recombination rate, U_s, for single-energy level surface states can be obtained as

$$U_s = \frac{n_s p_s - n_i^2}{\frac{n_s + n_1}{S_{p0}} + \frac{p_s + p_1}{S_{n0}}} \ , \tag{2.21}$$

where n_s and p_s are the electron and the hole *volume* concentrations at the surface and S_{n0} and S_{p0} are the characteristic surface recombination velocities of the surface states, which are related the surface states density, N_{st} (cm^{-2}) as:

$$S_{p0} \equiv \sigma_p v_{th} N_{st} \text{ and} \tag{2.22}$$

$$S_{n0} \equiv \sigma_n v_{th} N_{st} \quad . \tag{2.23}$$

Consequently, through the definition of the surface recombination velocity (Equation 2.20), the SRH surface recombination velocity can be obtained as

$$S = \frac{n_{s0} + p_{s0} + \Delta n}{\frac{n_s + n_1}{S_{p0}} + \frac{p_s + p_1}{S_{n0}}} \quad . \tag{2.24}$$

In reality, surface states are not localized at a single-energy level but are distributed across the band gap of a semiconductor. Here, the total surface recombination rate is obtained by integrating Equation 2.21 through the entire band gap of a semiconductor:

$$U_s = \int_{E_v}^{E_c} \frac{n_s p_s - n_i^2}{\frac{n_s + n_1(E)}{\sigma_p(E)} + \frac{p_s + p_1(E)}{\sigma_n(E)}} \cdot v_{th} \cdot D_{it}(E) \cdot dE \quad , \tag{2.25}$$

where E_v is the conduction band energy, E_c is the valence band energy, and D_{it} is the density of surface states per unit energy ($1/(eV \cdot cm^2)$).

2.3 Minority-Carrier Transport in a Semiconductor

In the previous sections, only the recombination activity in a certain volume or at a certain plane of a device was considered. To understand a device operation, however, all the activities that occur at different sites within a device need to be coupled with one another. It is the carrier transport process that connects these activities. This section gives a review of the theory of carrier transport in a semiconductor device.

For simplicity, one-dimensional carrier transport (along the x-axis) is considered. This is illustrated in Figure 2.7.

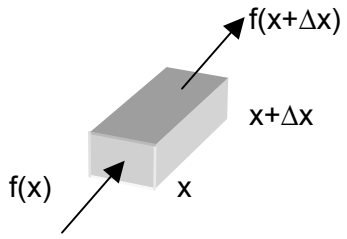


Figure 2.7 Schematic representation of one-dimensional carrier transport in an arbitrary system.

The system has an input flux of f(x) (1/(cm^2-s)), an output flux of f(x+Δx) (1/(cm^2-s)), a volume generation rate of G (1/(cm^3-s)), and a volume loss (recombination) rate of U_v (1/(cm^3-s)), the rate of change of a particle concentration in this volume (η) can be expressed as

$$\frac{d\eta}{dt} = \frac{f_\eta(x) - f_\eta(x+\Delta x)}{\Delta x} + G - U_V \text{ or} \tag{2.26}$$

$$\frac{d\eta}{dt} = -\frac{df_\eta(x)}{dx} + G - U_V \ . \tag{2.27}$$

This is the general form of the one dimensional continuity equation.

From the drift-diffusion theory (more detail derivation can be found in [15]), the flux of electrons and holes in a semiconductor can be described as

$$f_n = -\frac{J_n}{q} = -\left(n\mu_n \xi + D_n \frac{dn}{dx} \right) \text{ and} \tag{2.28}$$

$$f_p = +\frac{J_p}{q} = +\left(p\mu_p \xi - D_p \frac{dp}{dx} \right), \tag{2.29}$$

where, J_n and J_p are electrical current densities contributed by electrons and holes, μ_n and μ_p is the mobility of electrons and holes, D_n and D_p is the diffusivity of electrons and

holes, and ξ is the electric field. The electric field can be obtained through the Poisson equation:

$$\frac{d\xi}{dx} = \frac{\rho}{\varepsilon} \ , \tag{2.30}$$

where ε is the dielectric permittivity in the volume. For a semiconductor, the Poisson equation can be rewritten as:

$$\frac{d\xi}{dx} = \frac{q(p - n + N_D^+ + N_A^-)}{\varepsilon} \ . \tag{2.31}$$

The general forms of the continuity equation for electrons and holes in a semiconductor can then be obtained as:

$$\frac{dn}{dt} = \frac{d\left(n\mu_n \xi + D_n \frac{dn}{dx} \right)}{dx} + G - U_V \ \text{and} \tag{2.32}$$

$$\frac{dp}{dt} = \frac{d\left(-p\mu_p \xi + D_p \frac{dp}{dx} \right)}{dx} + G - U_V \ . \tag{2.33}$$

Based on these general forms of the continuity equation in a semiconductor, two special cases of carrier transport that are related to the operation of most solar cells, which are under low-level injection, are discussed below. These cases involve (1) minority-carrier transport across a field-free semiconductor and (2) minority-carrier transport across a potential step.

2.3.1 Minority-Carrier Transport and Surface Recombination Velocity across a Field-Free Region

Consider one-dimensional carrier transport in a semiconductor (from arbitrary surface to the other), where the following assumptions hold:

(a) The system is in a steady state

(b) The system is homogenous (constant doping, constant mobility)

(c) There is negligible carrier generation in the volume

(d) There is negligible electric field in the volume

These conditions represent minority-carrier *diffusion* in a semiconductor where the system is in a steady state, has constant doping across the volume, has a negligible amount of a potential gradient across the volume, and has negligible generation in the volume.

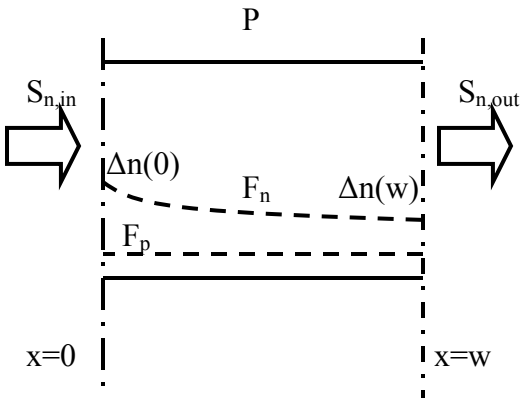


Figure 2.8 Energy band diagram representing electron diffusion in a homogenous field-free p-type semiconductor.

When electrons are injected into a p-type semiconductor, Figure 2.8, Equation 2.32 can be reduces to

$$\frac{d\left(D_n \frac{dn}{dx}\right)}{dx} = U_V \quad . \tag{2.34}$$

Assuming that the lifetime and the diffusivity are constant throughout the volume, Equation 2.34 can further be simplified to

$$D_n \frac{d^2(n_0 + \Delta n)}{dx^2} = \frac{\Delta n}{\tau_n} \quad \text{or} \tag{2.35}$$

$$D_n \frac{d^2(\Delta n)}{dx^2} = \frac{\Delta n}{\tau_n} \ . \tag{2.36}$$

The general solution of Equation 2.36 is as follows:

$$\Delta n(x) = c_1 \exp(\frac{x}{L_n}) + c_2 \exp(-\frac{x}{L_n}) \ , \tag{2.37}$$

where the definition of diffusion length, $L_n = \sqrt{D_n \cdot \tau_n}$ is implemented.

Two boundary conditions are required to obtain a specific solution. The most practical information is to find the input surface recombination velocity into this volume ($S_{n,in}$) as a function of the output surface recombination velocity ($S_{n,out}$) and the volume properties, which include the length (or the thickness) of the volume (w), the minority-carrier lifetime, and the minority-carrier diffusivity. Using the following two boundary conditions defined in terms of the surface recombination velocity,

$$f_n(0) = S_{n,in}\Delta n(0) = -D_n \left.\frac{d\Delta n}{dx}\right|_{x=0} \text{ and} \tag{2.38}$$

$$f_n(w) = S_{n,out}\Delta n(w) = -D_n \left.\frac{d\Delta n}{dx}\right|_{x=w} \ , \tag{2.39}$$

and by solving Equations 2.37-2.39, the input surface recombination velocity of electrons injected into a section of a field-free p-type semiconductor can be obtained as:

$$S_{n,in} = \frac{S_{n,out} + \frac{D_n}{L_n} \cdot \tanh(\frac{w}{L_n})}{1 + S_{n,out} \cdot \frac{L_n}{D_n} \cdot \tanh(\frac{w}{L_n})} \ . \tag{2.40}$$

Similarly, the input surface recombination velocity of holes injected into a field-free n-type semiconductor is:

$$S_{p,in} = \frac{S_{p,out} + \frac{D_p}{L_p} \cdot \tanh(\frac{w}{L_p})}{1 + S_{p,out} \cdot \frac{L_p}{D_p} \cdot \tanh(\frac{w}{L_p})} \ , \qquad (2.41)$$

where $L_p = \sqrt{D_p \cdot \tau_p}$ is the diffusion length of holes.

To provide insight on the physical meaning of Equations 2.40 and 2.41, two extreme cases are examined in further detail below.

(a) L<<w: the diffusion length is much smaller than the thickness

In this case, $\tanh\left(\frac{w}{L}\right)$=1 and Equations 2.40 and 2.41 become

$$S_{in} = \frac{D}{L} \ . \qquad (2.42)$$

This equation implies that when the diffusion length is much smaller than the thickness, the input surface recombination velocity is essentially equal to the bulk recombination velocity (D/L). Note that, in this case, because all carriers recombine before reaching the output surface, the recombination velocity at the output surface is not involved in the recombination process.

(b) L>>w: the diffusion length is much greater than the thickness

In this case, $\tanh\left(\frac{w}{L}\right)$=0 and Equations 2.40 and 2.41 become

$$S_{in} = S_{out} \ . \qquad (2.43)$$

This equation implies that when the diffusion length is much greater than the thickness, the input surface recombination velocity is essentially equal to the surface recombination velocity at the output plane. Note that because there are no or negligible

carriers recombine in the bulk, the bulk recombination is not involved in the recombination process.

Figure 2.9 shows the calculated surface recombination of electrons at the input plane as a function of the w/L ratio for three different recombination velocities at the output plane. As can be seen from the figure, the input and the output surface recombination velocities become equal (1,000 cm/s) when the w/L ratio becomes small (<0.007). On the other hand, the input recombination velocity becomes equal to the bulk recombination velocity when w/L becomes large (>3).

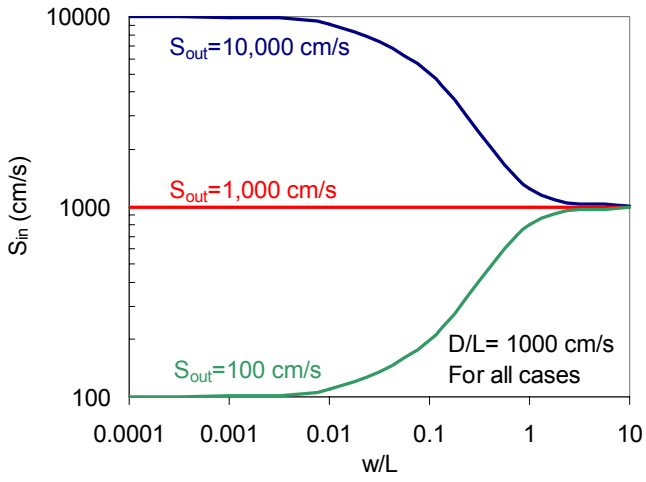


Figure 2.9 Surface recombination of electrons at the input plane of a homogenous field-free p-type semiconductor as a function of the w/L ratio for three different recombination velocities at the output plane: (a) 100 cm/s (b) 1,000 cm/s, and (c) 10,000 cm/s.

2.3.2 Minority-Carrier Transport and Surface Recombination Velocity across a Potential Gradient

Potential gradient in a semiconductor is typically formed in three ways: (1) external electrical bias, (2) impurity doping, and (3) fixed charge at the surface. Only the latter

two cases are discussed here, as they are more commonly related to the recombination in terrestrial solar cells.

The amount and the direction of the potential gradient can vary depending upon (1) the type of the majority carrier on each side of the grading region and (2) the amount of the concentration difference. Here, two forms of potential gradient that are commonly implemented for surface passivation in Si solar cells are discussed in detail: (1) a lo-hi junction (often referred to as a surface field) where a potential gradient is formed between two regions with the same type of majority carriers but with different magnitude (Figure 2.10) and (2) a floating p-n junction where the junction is formed between p- and n-regions (Figure 2.11). *Floating*, here, refers to the fact that this p-n junction is isolated from any external electrical bias.

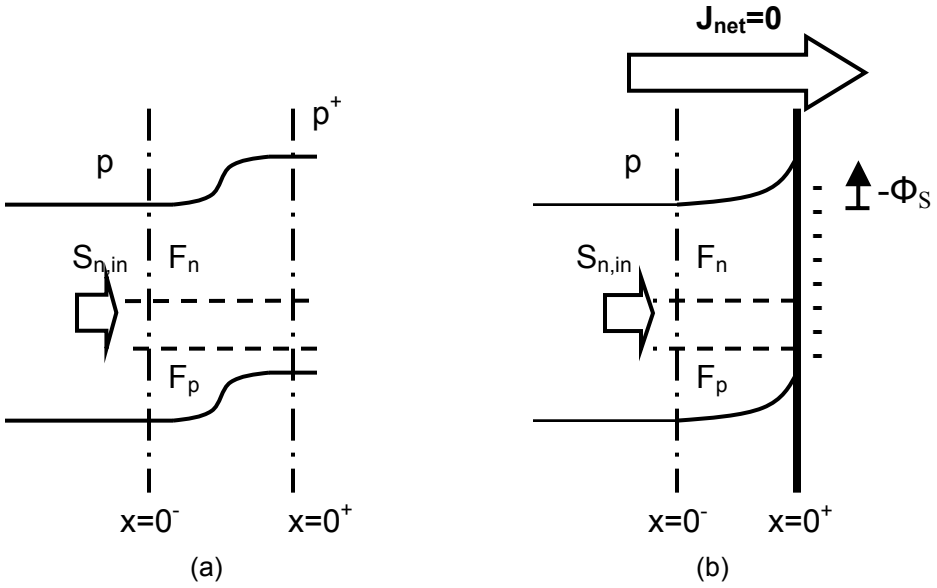


Figure 2.10 Energy band diagram of a surface field structure in a p-type substrate formed by (a) introduction of dopants and (b) presence of charge at the surface.

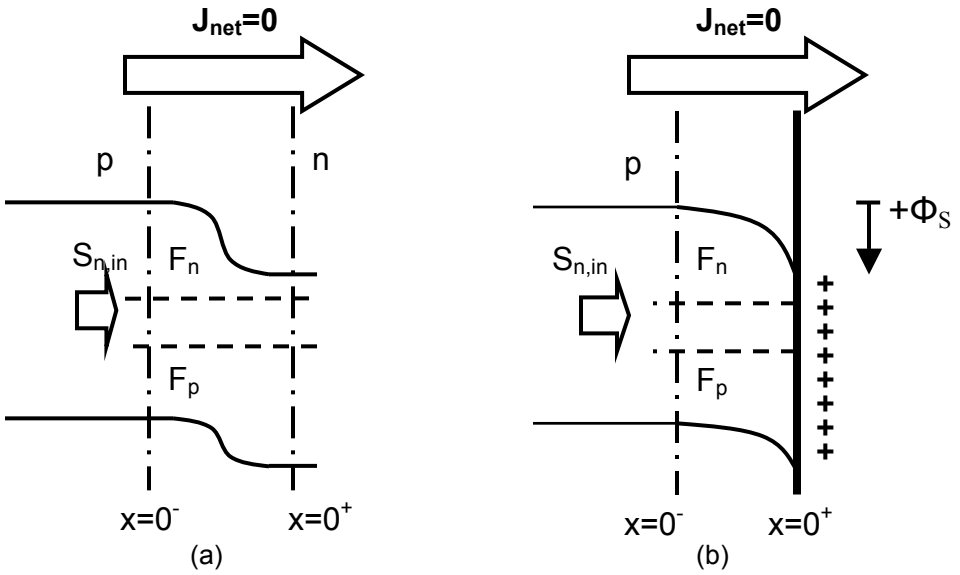


Figure 2.11 Energy band diagram of a floating-junction structure in a p-type substrate formed by (a) introduction of dopants and (b) presence of charge at the surface.

Here, the assumption of a constant Fermi level across the potential gradient [16] is used to simplify the problem. This assumption is valid when the following two conditions hold: (1) there is negligible generation and recombination within the field region and (2) the electrostatic potential difference across the field region resulted from the flow of carriers is negligible compared to that arising from the difference in the doping concentration or from the surface charge. This implied that the electron and the hole fluxes as well as the product of the electron and the hole concentrations stay constant across the field region:

$$f_n(0^-) = f_n(0^+) \text{ and } f_p(0^-) = f_p(0^+) \qquad \text{and} \qquad (2.44)$$

$$n(0^-) \cdot p(0^-) = n(0^+) \cdot p(0^+) \ . \qquad (2.45)$$

Additionally, if the output surface is free from any external electrical bias, i.e., the floating junction or the surface charge cases, there is no net current across the potential gradient. As a result,

$$f_n(0^+) = f_p(0^+) \qquad \text{(surface charge or floating junction)}, \qquad (2.46)$$

and this, combined with 2.44, gives

$$f_n(0^-) = f_n(0^+) = f_p(0^-) = f_p(0^+) \quad \text{(surface charge or floating junction)}. \qquad (2.47)$$

Using this concept, each of the four cases relevant to this research is analyzed in detail below.

2.3.2.1 Surface Recombination Velocity across Potential Gradient Introduced by Impurity Doping

2.3.2.1.1 Lo-Hi Junction

The lo-hi junction in a p-type semiconductor is shown in Figure 2.10a. Substituting for flux in terms of the recombination velocity, Equation 2.44 can be written as:

$$\Delta n(0^-) \cdot S_{n,in} = \Delta n(0^+) \cdot S_{n,out} \text{ or} \qquad (2.48)$$

$$S_{n,in} = \frac{\Delta n(0^+)}{\Delta n(0^-)} \cdot S_{n,out} \ . \qquad (2.49)$$

By assuming substantial injection in the volume ($\Delta n >> n_0$), Equation 2.45 can be written as:

$$\frac{\Delta n(0^+)}{\Delta n(0^-)} = \frac{p(0^-)}{p(0^+)} \ . \qquad (2.50)$$

Substitute Equation 2.50 into Equation 2.49:

$$S_{n,in} = \frac{p(0^-)}{p(0^+)} \cdot S_{n,out} \ . \qquad (2.51)$$

By further assuming low-level injection, an expression for the input surface recombination velocity as a function of the output surface recombination velocity for a lo-hi junction can be obtained as:

$$S_{n,in} = \frac{N_a(0^-)}{N_a(0^+)} \cdot S_{n,out} \ . \tag{2.52}$$

Equation 2.52 indicates that a lo-hi doping step reduces the surface recombination velocity of the minority carrier at the input plane by the ratio of the low-to-high doping concentration. A higher step results in a lower recombination velocity.

2.3.2.1.2 Floating Junction

A floating junction in a p-type semiconductor is shown in Figure 2.11a. Again, by substituting for flux in terms of the recombination velocity, Equation 2.47 can be written as:

$$\Delta n(0^-) \cdot S_{n,in} = \Delta p(0^+) \cdot S_{p,out} \qquad \text{or} \tag{2.53}$$

$$S_{n,in} = \frac{\Delta p(0^+)}{\Delta n(0^-)} \cdot S_{p,out} \ . \tag{2.54}$$

By assuming substantial injection in the volume ($\Delta n >> n_0$ in the p-region $\Delta p >> p_0$ in the n-region), Equation 2.45 can be written as:

$$\frac{\Delta p(0^+)}{\Delta n(0^-)} = \frac{p(0^-)}{n(0^+)} \ . \tag{2.55}$$

Substitute Equation 2.55 into Equation 2.54:

$$S_{n,in} = \frac{p(0^-)}{n(0^+)} \cdot S_{p,out} \ . \tag{2.56}$$

By further assuming low-level injection, an expression for the input surface recombination velocity as a function of the output surface recombination velocity for a floating junction is obtained as:

$$S_{n,in} = \frac{N_a(0^-)}{N_d(0^+)} \cdot S_{p,out} \ . \tag{2.57}$$

Similar to a lo-hi junction, Equation 2.57 indicates that a doping step (although with different polarity) reduces the surface recombination velocity at the input plane by the ratio of the base-to-floating junction doping concentration. Note, however, that the recombination velocity on the right hand side of the equation is the recombination velocity of holes.

2.3.2.1.3 Effect of Band Gap Narrowing on the Surface Recombination Velocity across Lo-Hi and Floating Junctions

To improve the accuracy of Equations 2.52 and 2.57, the band gap narrowing effect should be taken into account. This effect has an impact at high doping, where the band gap effectively becomes smaller with the increase in the doping concentration. This effect causes n_i to be doping dependent. To take into account this effect, Equation 2.45 should first be rewritten as

$$\frac{n(0^-)\cdot p(0^-)}{n_i^2(0^-)} = \frac{n(0^+)\cdot p(0^+)}{n_i^2(0^+)} \quad . \tag{2.58}$$

Consequently, Equations 2.50 and 2.55 become

$$\frac{\Delta n(0^+)}{\Delta n(0^-)} = \frac{p(0^-)}{p(0^+)}\cdot\frac{n_i^2(0^+)}{n_i^2(0^-)} \qquad \text{or} \qquad \frac{\Delta p(0^+)}{\Delta n(0^-)} = \frac{p(0^-)}{n(0^+)}\cdot\frac{n_i^2(0^+)}{n_i^2(0^-)} \quad , \tag{2.59}$$

respectively.

The n_i^2 ratio can be expressed in terms of the magnitude of the band gap narrowing on the left plane ($\Delta V_G(0^-)$) and the right plane ($\Delta V_G(0^+)$) as

$$\frac{n_i^2(0^+)}{n_i^2(0^-)} = \exp\left[\frac{q(\Delta V_G(0^+) - \Delta V_G(0^-))}{kT}\right] . \tag{2.60}$$

The input surface recombination velocity of a lo-hi junction can then be expressed as

$$S_{n,in} = \frac{N_a(0^-)}{N_a(0^+)} \cdot \exp\left[\frac{q(\Delta V_G(0^+) - \Delta V_G(0^-))}{kT}\right] \cdot S_{n,out} \quad . \qquad (2.61)$$

Similarly, the input surface recombination velocity for a floating junction can then be expressed as

$$S_{n,in} = \frac{N_a(0^-)}{N_d(0^+)} \cdot \exp\left[\frac{q(\Delta V_G(0^+) - \Delta V_G(0^-))}{kT}\right] \cdot S_{p,out} \quad . \qquad (2.62)$$

As can be seen from Equations 2.61 and 2.62, the band gap narrowing works against the reduction of the surface recombination velocity.

2.3.2.2 Surface Recombination Velocity across Potential Gradient Introduced by Surface Charge

For the potential gradient formed by surface charge, both lo-hi and floating junctions can be treated using the same set of equations. Therefore, the two cases of surface charge shown in Figure 2.10b and Figure 2.11b are dealt at the same time.

The electron and hole concentrations at the surface can be obtained as a function of the surface potential (Φ_S) according to

$$n(0^+) = n(0^-) \cdot \exp\left(\frac{+\Phi_S}{kT}\right) \text{ and} \qquad (2.63)$$

$$p(0^+) = p(0^-) \cdot \exp\left(\frac{-\Phi_S}{kT}\right) . \qquad (2.64)$$

The surface potential can be obtained by applying the charge neutrality condition at or in the vicinity of the Si surface. One of the techniques used in obtaining the surface potential as a function of surface charge can be found in [17] and will not be covered here.

For substantial injection ($\Delta n >> n_0$), Equation 2.63 and 2.64 can be expressed as

$$n(0^+) = \Delta n(0^-) \cdot \exp\left(\frac{+\Phi_S}{kT}\right) \text{ and} \tag{2.65}$$

$$p(0^+) = \left[N_a(0^-) + \Delta n(0^-)\right] \cdot \exp\left(\frac{-\Phi_S}{kT}\right). \tag{2.66}$$

Because there is no electrical connection to the surface plane on the right surface (see also Figure 2.10b and Figure 2.11b), the electron and hole fluxes to the surface must be equal. Furthermore, based on the assumption put forth earlier that there is negligible recombination in the field region, it follows that the electron and the hole fluxes to the surface become equal to the recombination rate at the surface, U_s, which can be obtained through the surface SRH theory (Equation 2.21 or 2.25). Consequently, Equation 2.47 can be expressed as

$$f_n(0^-) = f_p(0^-) = \frac{n(0^+)p(0^+) - n_i^2}{\frac{n(0^+) + n_1}{S_{p0}} + \frac{p(0^+) + p_1}{S_{n0}}}, \tag{2.67}$$

where $n(0^+)$ and $p(0^+)$ can be obtained using Equation 2.65 and 2.66, respectively. The expression for the input surface recombination velocity for a potential gradient formed by surface charge can then be calculated from

$$S_{n,in} = \frac{f_n(0^-)}{\Delta n(0^-)} = \frac{1}{\Delta n(0^-)} \cdot \left[\frac{n(0^+)p(0^+) - n_i^2}{\frac{n(0^+) + n_1}{S_{p0}} + \frac{p(0^+) + p_1}{S_{n0}}}\right]. \tag{2.68}$$

2.3.3 Reverse Saturation Current Density

Another important quantity that is often used to characterize minority-carrier transport in a semiconductor is the reverse saturation current density (J_0). In general, J_0

can be assigned to any arbitrary plane the same way as the surface recombination velocity.

The concept of J_0 is introduced primarily to describe the current flow in a p-n junction diode. Therefore it is instructive to begin the derivation by examining the current flow in such a diode. A schematic of a p-n junction diode under forward bias of V_A volt is shown in Figure 2.12.

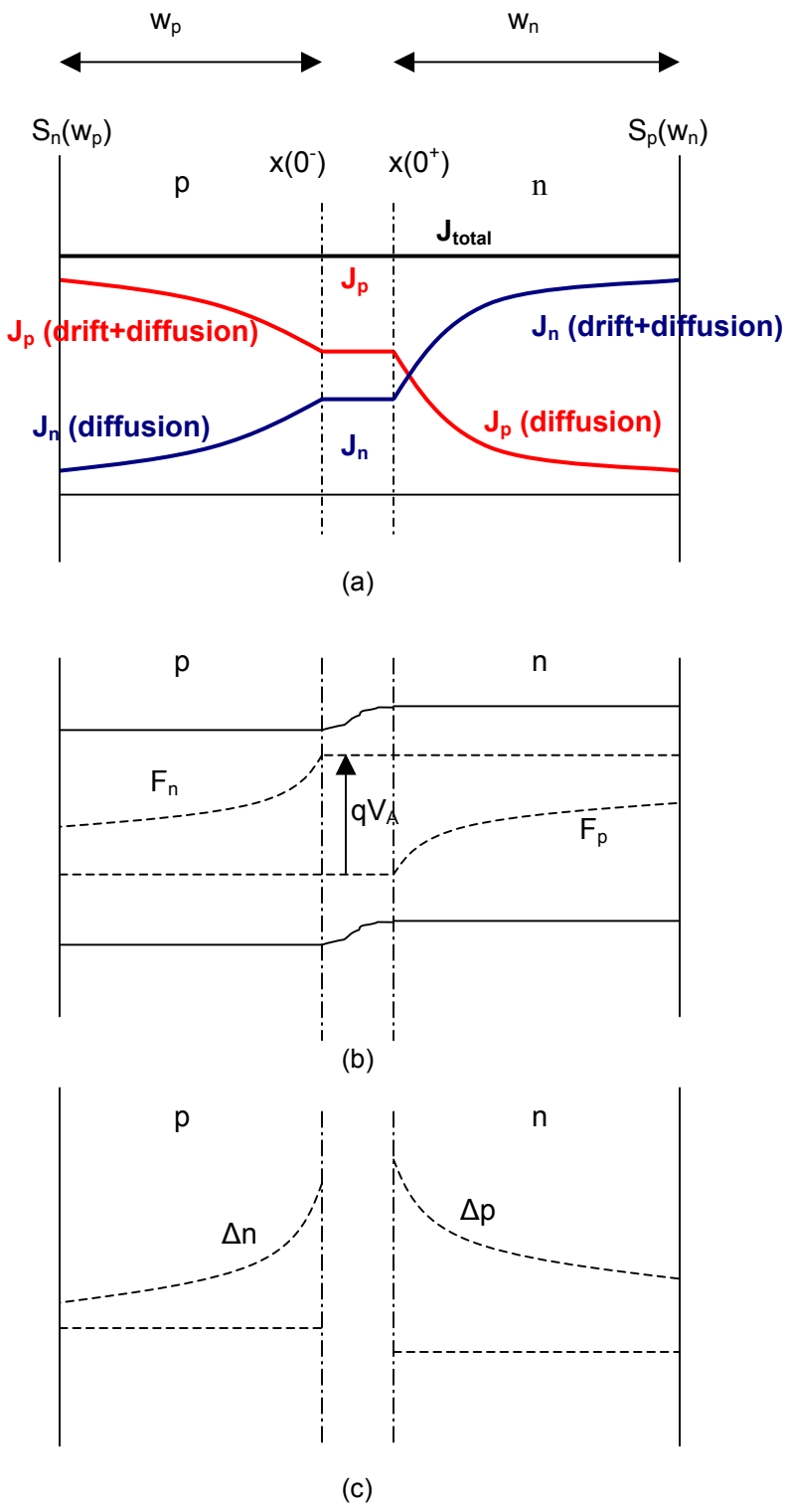


Figure 2.12 p-n junction under a forward bias condition: (a) current density, (b) energy band diagram, and (c) minority-carrier concentration.

Forward bias of a p-n junction lowers the potential barrier that prevents electrons and holes from diffusing from n- to p-side and p- to n-side, respectively. The electrons and holes those are able to diffuse across the junction become minority carriers on the other side. These injected minority carriers recombine with the majority carriers supplied by the contact, resulting in a current flow. Assuming negligible recombination inside the depletion region leads to the following conditions:

- The current stays constant across the depletion region and
- The quasi-Fermi level stays constant inside the depletion region and the separation between the electron and the hole quasi-Fermi levels is equal to the applied voltage

The first condition allows the calculation of the total current by simply adding the minority-carrier current on each side of the junction edge (Figure 2.12a):

$$J_{total}=J_n(0^+)+J_p(0^-)\ . \tag{2.69}$$

The second condition allows determination of the carrier concentration at the edge of the depletion region according to the law of junction:

$$n_p(0^-) = n_{p0}\cdot\exp\left(\frac{F_n(0^-)-F_p(0^-)}{kT}\right)= n_{p0}\cdot\exp\left(\frac{q\cdot V_A}{kT}\right) \text{ and} \tag{2.70}$$

$$p_n(0^+) = p_{n0}\cdot\exp\left(\frac{F_n(0^+)-F_p(0^+)}{kT}\right) = p_{n0}\cdot\exp\left(\frac{q\cdot V_A}{kT}\right), \tag{2.71}$$

where n_{p0} and p_{n0} are electron and hole concentrations in the p- and n-sides at equilibrium, respectively.

Flux of electrons injected into the p-side can be calculated from the recombination velocity according to

$$J_n(0^-) = -q \cdot f_n(0^-) = -q \cdot S_n(0^-) \cdot \Delta n(0^-) = -q \cdot S_n(0^-) \cdot [n_p(0^-) - n_{p0}]. \quad (2.72)$$

By assuming low-level injection, it follows that the minority-carrier current is composed only of the diffusion current (no drift or field component). Consequently, this scenario becomes essentially the same scenario as the one shown in Figure 2.8 (electrons injected into a homogenous field-free p-type semiconductor); therefore, the input surface recombination velocity $S_n(0^-)$ can be obtained directly from Equation 2.40 as

$$S_n(0^-) = -\left[\frac{S_n(w_p) + \frac{D_n}{L_n} \cdot \tanh\left(\frac{w_p}{L_n}\right)}{1 + S_n(w_p) \cdot \frac{L_n}{D_n} \cdot \tanh\left(\frac{w_p}{L_n}\right)} \right]. \quad (2.73)$$

Substituting $S_n(0^-)$ from Equation 2.73 and $n_p(0^-)$ from Equation 2.70 into Equation 2.72, $J_n(0^-)$ can then be obtained as:

$$J_n(0^-) = q \cdot \left[\frac{S_n(w_p) + \frac{D_n}{L_n} \cdot \tanh\left(\frac{w_p}{L_n}\right)}{1 + S_n(w_p) \cdot \frac{L_n}{D_n} \cdot \tanh\left(\frac{w_p}{L_n}\right)} \right] \cdot \left\{ n_{p0} \cdot \left[\exp\left(\frac{q \cdot V_A}{kT}\right) - 1 \right] \right\}. \quad (2.74)$$

Similarly, fcurrent contributed by the flow of holes at the junction edge of the n-side can be expressed as:

$$J_p(0^+) = q \cdot \left[\frac{S_p(w_n) + \frac{D_p}{L_p} \cdot \tanh\left(\frac{w_n}{L_p}\right)}{1 + S_p(w_n) \cdot \frac{L_p}{D_p} \cdot \tanh\left(\frac{w_n}{L_p}\right)} \right] \cdot \left\{ p_{n0} \cdot \left[\exp\left(\frac{q \cdot V_A}{kT}\right) - 1 \right] \right\}. \quad (2.75)$$

The total current can then be obtained by adding Equation 2.74 and 2.75:

$$J_{total} = q \cdot \left[p_{n0} \frac{S_p(w_n) + \frac{D_p}{L_p} \cdot \tanh\left(\frac{w_n}{L_p}\right)}{1 + S_p(w_n) \cdot \frac{L_p}{D_p} \cdot \tanh\left(\frac{w_n}{L_p}\right)} + n_{p0} \frac{S_n(w_p) + \frac{D_n}{L_n} \cdot \tanh\left(\frac{w_p}{L_n}\right)}{1 + S_n(w_p) \cdot \frac{L_n}{D_n} \cdot \tanh\left(\frac{w_p}{L_n}\right)} \right] \cdot$$

$$\left[\exp\left(\frac{q \cdot V_A}{kT}\right) - 1 \right] \tag{2.76}$$

The reverse saturation current density is defined as the current under a reverse bias. In such a case, exp (qV_A/kT) ~0 and, therefore, from Equation 2.76, J_0 can be expressed as

$$J_0 = q \cdot \left[p_{n0} \frac{S_p(w_n) + \frac{D_p}{L_p} \cdot \tanh\left(\frac{w_n}{L_p}\right)}{1 + S_p(w_n) \cdot \frac{L_p}{D_p} \cdot \tanh\left(\frac{w_n}{L_p}\right)} + n_{p0} \frac{S_n(w_p) + \frac{D_n}{L_n} \cdot \tanh\left(\frac{w_p}{L_n}\right)}{1 + S_n(w_p) \cdot \frac{L_n}{D_n} \cdot \tanh\left(\frac{w_p}{L_n}\right)} \right]. \tag{2.77}$$

This represents the reverse saturation current density for a simple p-n junction diode with homogeneous emitter and base under low-level injection. Substituting J_0 into Equation 2.76 provides a basic diode equation:

$$J_{total} = J_0 \cdot \left[\exp\left(\frac{q \cdot V_A}{kT}\right) - 1 \right]. \tag{2.78}$$

Note that J_0 is related to the recombination velocity of the minority carriers at the two junction edges as follows:

$$J_0 = q \cdot (p_{n0} \cdot S_{p,in} + n_{p0} \cdot S_{n,in}), \tag{2.79}$$

where $S_{p,in}$ and $S_{n,in}$ are the hole and the electron recombination velocities at the junction edges on the n and p-sides, respectively.

Assuming that n_i at the two junction edges is equal (no band gap narrowing), Equation 2.79 can be written as:

$$J_0 = q \cdot n_i^2 \cdot \left(\frac{1}{N_D} \cdot S_{p,in} + \frac{1}{N_A} \cdot S_{n,in} \right). \tag{2.80}$$

For p-type based Si solar cells, J_0 is normally subdivided into emitter saturation current density (J_{0e}) and base saturation current density (J_{0b}), where:

$$J_{0e} = q \cdot \frac{n_i^2}{N_D} \cdot S_{p,in} \; and \; J_{0b} = q \cdot \frac{n_i^2}{N_A} \cdot S_{n,in}. \tag{2.81}$$

J_0 can also be expressed in terms of the n-p product at any plane within the device:

$$J = J_0 \cdot \left[\exp\left(\frac{q \cdot V}{kT} \right) - 1 \right] = J_0 \cdot \left[\exp\left(\frac{F_n - F_p}{kT} \right) - 1 \right] = J \cdot \left(\frac{np}{n_i^2} - 1 \right) \tag{2.82}$$

This expression is especially useful in dealing with a device under high-level injection.

CHAPTER 3

BACK SURFACE PASSIVATION TECHNIQUES AND STRUCTURES FOR P-TYPE SI SOLAR CELLS

Surface passivation is used to minimize electron-hole pair recombination at the surface of semiconductor devices. Surface passivation is extremely important in solar cells as any loss (or recombination) of photogenerated carriers translates directly into loss in cell performance. This chapter provides a review of back surface passivation for p-type Si solar cells. First, common techniques used to passivate the back surface of p-type Si solar cells are discussed, followed by examples of high-efficiency p-type Si solar cell structures that incorporate high-quality back surface passivation.

3.1 Techniques for Back Surface Passivation for p-Type Si Solar Cells

Back surface passivation techniques are categorized into two groups: (1) an introduction of dopants to inhibit carrier transport to the surface and (2) a deposition or a growth of dielectric layers on the surface to reduce the surface state density.

3.1.1 Introduction of Dopants to Inhibit Carrier Transport to the Surface to Provide Surface Passivation

As discussed in Chapter 2, a formation of either a BSF or a floating junction can be used to prevent carriers from reaching the surface and recombine. This section gives a short review of common dopants and techniques used to obtain these structures.

3.1.1.1 Al-BSF

When the first p-type BSF Si cell was introduced in 1972, Al doping was used to form the BSF [18]. Through research and development, the Al-BSF process has been simplified from Al evaporation followed by a four-hour long anneal to screen-printing of thick-paste Al followed by a few seconds in-line anneal in a belt furnace. The screen-printed Al-BSF is currently the most widely used technique for back surface passivation of p-type Si solar cells. Its popularity is attributed to its simplicity, low cost, and high-throughput capability.

The formation of an Al-BSF by a screen-printing process involves two steps: (1) full-area screen-printing of an Al paste on the back surface followed by (2) a short anneal above the Al-Si eutectic temperature (577°C). During the 700-900°C anneal, Si is dissolved into an Al-Si alloy melt. During the cool-down, Si is rejected from the melt and is regrown on the surface as an Al-doped p^+ BSF layer [19]. A simple schematic of the process is shown in Figure 3.1. Because of the nature of the process, an electrical contact is obtained on top of the BSF region without any additional step.

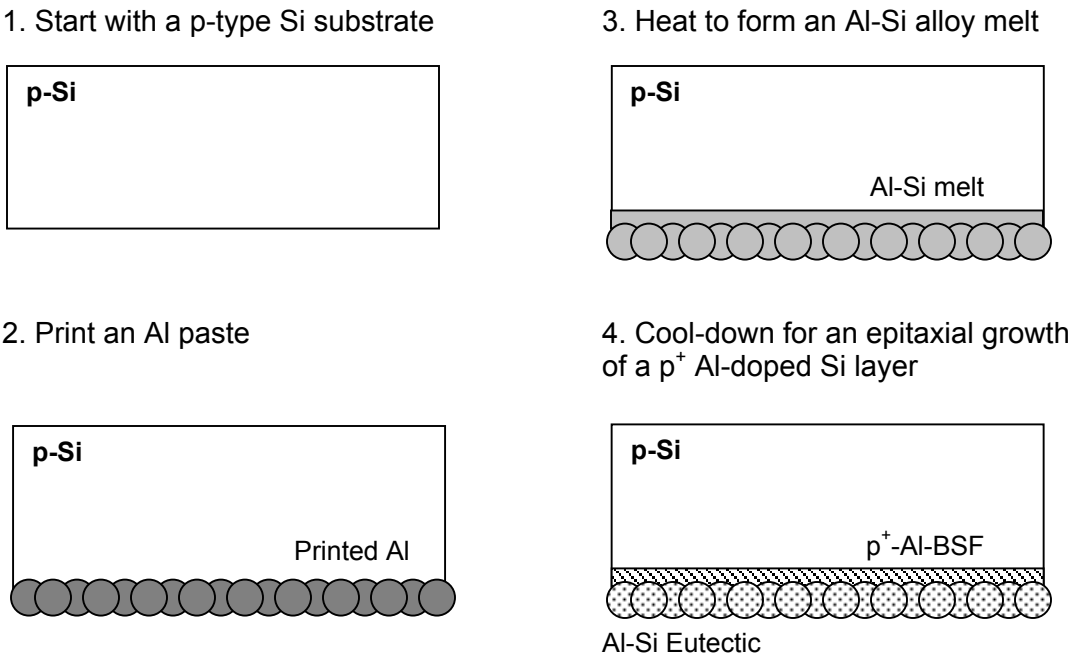


Figure 3.1 Schematic representation of the Al-BSF formation by a screen-printing process.

The thickness of the Al-BSF layer is determined by the amount of Si dissolved into the Al-Si melt at the peak temperature. The amount of dissolved Si is dictated by the deposited Al thickness and the peak alloying temperature, in accordance with the phase diagram of the Al-Si binary system (Figure 3.2a). The BSF thickness or the p-p^+ junction depth can be expressed as follows [20]:

$$W_{BSF} = \frac{t_{Al} \cdot \rho_{Al}}{\rho_{Si}} \left(\frac{F(T)}{1-F(T)} - \frac{F(T_0)}{1-F(T_0)} \right), \tag{3.1}$$

where t_{Al} represents the thickness of the deposited or printed Al layer, ρ_{Si} and ρ_{Al} are the densities of Si and Al (porosity should be taken into account), $F(T)$ represents the atomic percentage of Si in the molten phase at the peak alloying temperature, and $F(T_o)$ represents the Si atomic percentage at the eutectic temperature (~ 12.2% from the phase diagram in Figure 3.2a).

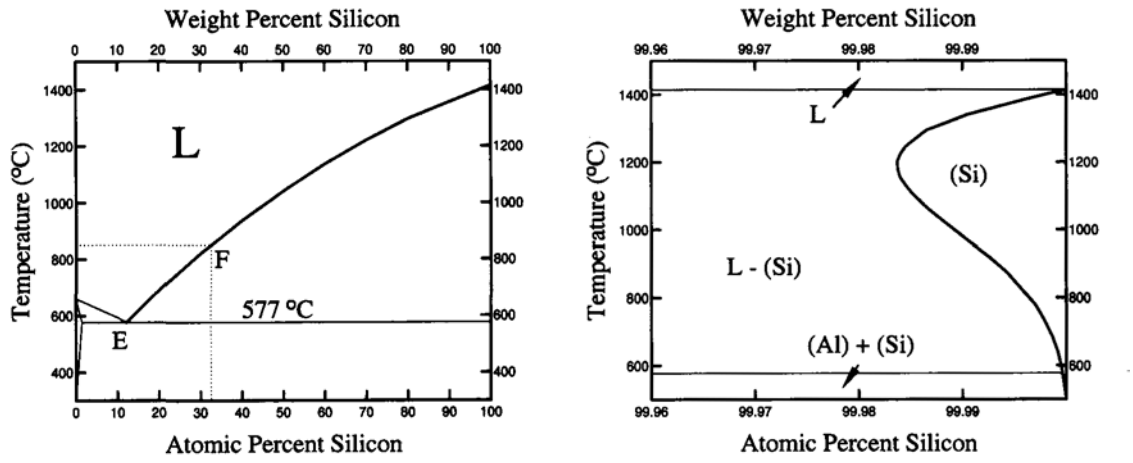


Figure 3.2 Phase diagram of the Al-Si binary system (taken from [21], originally from [22]): (a) the overall phase diagram, (b) the close-up on the solid-solubility of Al in Si.

The doping profile of the Al-BSF layer is, to the first order, governed by the Al-Si phase diagram. As previously mentioned, during the cool-down process, the excess Si is rejected from the melt and re-grows epitaxially at the Si-liquid interface. This re-growth layer is doped with Al according to the solidus line (Figure 3.2b), which delineates the solid solubility of Al in Si as a function of the re-growth temperature. The solid solubility of Al in Si decreases with the decrease in the temperature below 1,200° C (Figure 3.2b), resulting in a retrograde Al profile with a decreasing Al concentration from the p-p^+ interface to the rear Al contact (Figure 3.3). Theoretically, according to the phase diagram in Figure 3.2b, the Al-doped BSF layer should have a peak concentration in the range of 1-3×10^{18} cm^{-3} at the p-p^+ interface for a peak alloying temperature in the range of 750-900°C, which is typical for the screen-printed Al-BSF process. For most p-type Si solar cells, the base doping concentration is generally much lower (<2×10^{16} cm^{-3}), resulting in a lo-hi junction for surface passivation.

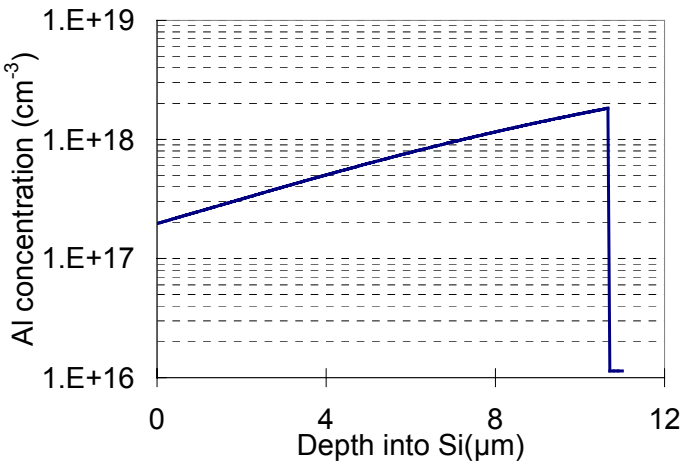


Figure 3.3 Calculated Al-doping profile by the Al-Si alloying process (for a deposited Al thickness of 35 μm and a peak alloying temperature of 800°C).

In spite its simplicity; the screen-printed Al-BSF process has its drawbacks. Even though a surface recombination velocity as low as 200 cm/s on 2-3 ohm-cm Si has been demonstrated using the screen-printed Al-BSF [19, 23], such a value is often difficult to reproduce and is still unable to meet the requirement for achieving a 20% efficient cell, which is the target for the PV industry [24]. The internal back surface reflection is also found to be low to moderate (65-80%) [25-28]. Finally, the Al-Si alloying process induces stress to the Si substrate because of the difference in the thermal expansion coefficient between Al and Si [29, 30]. All of these drawbacks become more critical in thinner Si cells.

3.1.1.2 B-BSF

Boron is another key dopant for the formation of a BSF for p-type Si solar cells. An introduction of B into Si is typically done through a diffusion process (as opposed to an alloying process for the Al-BSF). In general, a B_2O_3 compound is first formed on the Si

surface. Subsequently, at an elevated temperature, B_2O_3 reacts with the underlying Si to form SiO_2 and elemental B according to

$$2B_2O_3 + 3Si \rightarrow 3SiO_2 + 4B \quad . \tag{3.2}$$

Because of the moderately low diffusion coefficient [31], the B-diffusion is normally performed at high temperatures (>1,000°C). The B-diffusion can be achieved with gaseous, liquid, and solid sources.

The benefits of using the B-BSF are that it provides the passivation of the back surface and simplifies the formation of an ohmic contact on high resistivity substrates because of the high B doping concentration at the surface. The B-BSF is also compatible with subsequent dielectric passivation, which further enhances the passivation and the optical qualities of the back surface. However, the main challenge for the implementation of the B-BSF lies in the process control to diffuse B without degrading the bulk minority-carrier lifetime in Si. Although B-doping of Si during Si growth is very well established and gives an exceptionally high bulk lifetime, several studies have shown that diffusion of B into Si substrates requires extra attention to both the cleanliness and the process parameters to preserve the carrier lifetime [32-35]. Some researchers attribute the lifetime degradation during the B-BSF formation to the injection of metallic impurities into the substrate [32], while others propose that diffusion of B induces stress and point defects on the surface [34], which lead to the formation of dislocations during the diffusion itself or in a subsequent high-temperature process. It was also shown in [36] that the presence of Fe, one of the most common metallic impurities in Si solar cells, is more detrimental in the B-diffused layer than in the P-diffused layer. Nevertheless, several research groups have been able to maintain the high minority-carrier lifetime (≥ 1ms) through the B-

diffusion process using excellent process control [35, 37, 38]. It should be noted that all the high lifetimes reported were obtained using either gaseous or liquid B-sources.

3.1.1.3 P Floating Junction

Phosphorus is the primary dopant used in Si solar cells for n-type doping. Because of its relatively high diffusion coefficient in Si [31], P can be diffused at a relatively low temperature (below 900°C). Similar to the B-diffusion process, a P_2O_5 compound is first formed on the Si surface. It then reacts with the underlying Si at an elevated temperature to form SiO_2 and elemental P according to

$$2P_2O_5 + 5Si \rightarrow 5SiO_2 + 4P \quad . \qquad (3.3)$$

P-diffusion can also be achieved with gaseous, liquid, and solid sources. However, unlike B, P-diffusion was found to be much more forgiving in terms of the cleanliness of the diffusion process.

The back surface passivation of p-type Si solar cells by an n-type floating-junction layer was proposed in [39]. A solar cell with an open circuit voltage (V_{oc}) of 720 mV was reported in the laboratory using such a structure [40]. The challenge of applying the floating junction on commercial solar cells lies in the development of a simple process to maintain the junction as floating (electrically isolated from the back contact). Shunting of the floating junction by the back contact results in significant degradation in cell performance [40-43]. This requirement often leads to a more complicated process, which results in a higher cell fabrication cost.

3.1.2 Deposition or Growth of Dielectric Layers on the Si Surface to Minimize the Surface State Density

Since dielectric passivation is an important part of this thesis, in this section, various types of layers for Si surface passivation are reviewed. These include thermally grown SiO_2, PECVD SiN_x, PECVD SiC_x, and PECVD a-Si:H.

3.1.2.1 Thermally Grown SiO_2

The use of thermally grown SiO_2 on Si has been extensively studied and understood since the 1960s. Oxidation of Si is a natural process and can be controlled quite precisely. The interface quality obtained by such a process is superb, where as low as 10^9 $cm^{-2}eV^{-1}$ can be achieved, which corresponds to only one surface state per 10^5 Si surface atoms, [44]. In fact, the record high efficiency Si solar cell (24.7%) utilizes thermally grown SiO_2 for passivation of both front and back surfaces [45]. However, to obtain a high passivation quality, oxidation needs to be conducted at a high temperature (>1000°C) [46] in a clean environment. The high-temperature requirement is relaxed if a wet oxidation process (H_2O as a precursor) is used rather than a dry oxidation process (O_2 as a precursor). An additional treatment such as a 350-500°C anneal in a hydrogen-containing ambient (a forming gas anneal (FGA)) or, even more effectively, with an evaporated Al capping layer (so called “alneal” [47]) is normally applied to achieve a very low surface state density [46, 48] (Figure 3.4).

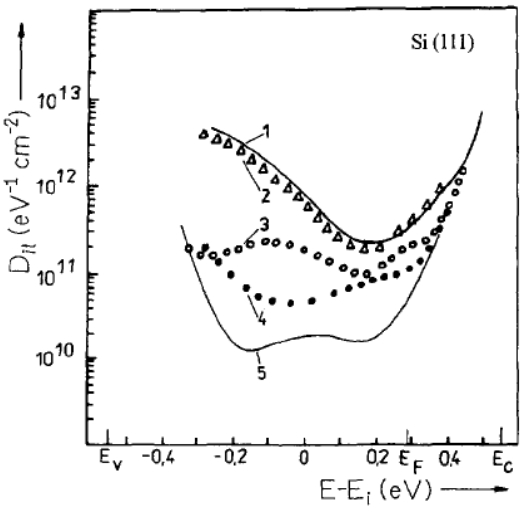


Figure 3.4 Effect of a low temperature anneal (450°C, 30 minutes) on the surface state density (D_{it}) at Si/SiO_2 interface [48]. Curve 1: as-oxidized, Curve 2: annealed in dry N_2 before Al evaporation, Curve 3: annealed in a forming gas before Al evaporation, Curve 4: post Al-metallization (partial Al coverage) annealed in a forming gas; Curve 5: post Al-metallization (full Al coverage) annealed in a forming gas.

One of the main limitations of thermally grown SiO_2 is its poor thermal stability during a subsequent high-temperature process. This inhibits the incorporation of SiO_2 passivation to the existing screen-printing contact technology, where a short anneal at a moderately high temperature (750°C-850°C) in a breathing air is required to form a contact.

3.1.2.2 PECVD-SiN_x

The PECVD SiN_x is extensively used in PV industry today for antireflection coating on the front surface. It also provides good surface passivation for the n-type emitter of p-type Si solar cells [49, 50] and can be deposited at a relatively low temperature (300-450°C). The use of PECVD SiN_x for back surface passivation has recently gained a lot of attention. It has not worked yet for p-type Si because of the formation of an inversion layer by the high positive charge in the SiN_x layer (PECVD SiN_x has a high positive charge density of 1×10^{11} to 5×10^{12} cm^{-2} as opposed to 5×10^{10} to 2×10^{11} cm^{-2} for

thermally grown SiO_2 [44]). Similar to the floating junction, care must be taken to prevent electrical connection between the back contact and the inversion layer. Another concern about PECVD SiN_x is its thermal stability during a subsequent high-temperature step. However, it has been shown that a stack of thin (100 Å) thermally grown SiO_2 capped with PECVD SiN_x is thermally stable [51, 52], and can avoid the formation of a strong-inversion layer [53].

3.1.2.3 PECVD-SiC_x

Recently, PECVD SiC_x has gained momentum for use as a back surface passivation layer for p-type Si solar cells [54]. Very low surface recombination velocities, below 5 cm/s on 1.0 ohm-cm p-type Si, were demonstrated in [55]. It was also found that the SiC surface passivation could be maintained after a short anneal at 800°C by optimizing the chemical composition of the layer. Additionally, doping SiC_x with B was found to improve the passivation quality on a heavily B-doped surface for the B-BSF structure [56].

3.1.2.4 PECVD-amorphous-Si:H

Hydrogenated amorphous Si was found to provide an exceptionally low surface recombination velocity of 3 cm/s on a 1.6 ohm-cm p-type substrate [57]. The optimum temperature for the deposition was also found to be very low (~200-250°C). However, the thermal stability was found to be poor, which makes compatibility with the existing screen-printing technology, which uses > 700°C firing temperatures, less than promising. As a result, a new manufacturable technique for high-quality high-throughput contact formations still needs to be developed for low-cost high-efficiency commercial Si solar cells.

3.2 High-Efficiency Si Solar Cell Structures with Dielectric Back Passivation and Local Back Contacts

Many high-efficiency Si solar cell structures have been proposed and demonstrated in the literature that utilize a dielectric layer for back surface passivation. Four common structures are reviewed in this section. It should be noted that almost all these structures employ a metal layer on top of the dielectric layer. Such a dielectric/metal system behaves like an internal optical mirror on the back surface that provides a very high internal back surface reflection. Moreover, if a SiO_2/Al system is used, an alneal process can be utilized to improve the passivation quality.

3.2.1 Structure I: Dielectric Back Surface Passivation Without a BSF under the Local Back Contact

This represents the simplest structure for utilizing dielectric back passivation for Si solar cells. This structure requires three main process steps: (1) deposition or growth of a dielectric layer, (2) local openings through the dielectric layer, and (3) a metal/Si contact formation through the openings. An example of such a structure is the passivated emitter and rear cell (PERC) developed by the University of New South Wales (UNSW), which achieved an efficiency of 22.8% on a 0.2 ohm-cm p-type Si substrate (Figure 3.5) [58]. To achieve surface passivation in the PERC structure, a SiO_2 layer (~1000 Å) was thermally grown on both front and back surfaces. The local back contact was formed by opening the windows through the back SiO_2 layer using a photolithography process, followed by full-area Al evaporation. Subsequently, an FGA at 400°C was employed to form an ohmic contact and to improve the passivation quality. The weakness of such a simplified structure is the high recombination at the contact interface, which, in turn, puts a tight restriction on the contact-area fraction. Since the contact is made directly to the Si

substrate, the resistivity of the substrate needs to be below 1 ohm-cm to a attain good ohmic contact [35].

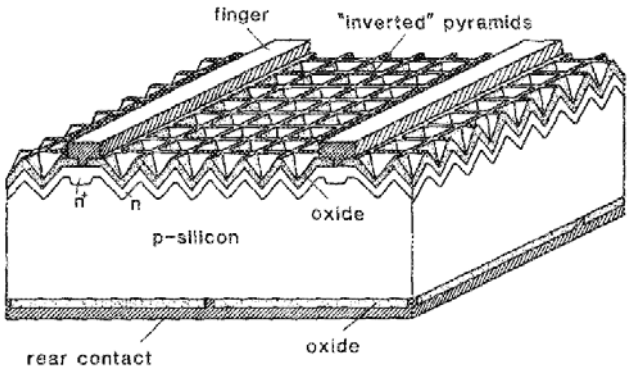


Figure 3.5 Example of a dielectric back-passivated cell structure without a BSF under the local contact: PERC cell [58].

3.2.2 Structure II: Dielectric Back Surface Passivation with a BSF under the Local Back Contact

The passivated emitter, rear locally diffused (PERL) cell was developed at UNSW and resulted in a record high terrestrial efficiency of 24.7% [35, 45, 59] (Figure 3.6). The back structure of the PERL cell includes a local B-BSF around the local back contacts, while thermally grown SiO_2 passivates the back surface elsewhere. The incorporation of a LBSF minimizes the recombination at the back contact and allows an ohmic contact on high-resistivity substrates. The fabrication of this local B-BSF cell, however, requires a lengthy process with several masking and high-temperature process steps, including (1) growth of thermal SiO_2 that serves as a B-diffusion mask, (2) photolithography process to define BSF windows, (3) B-diffusion using a BBr_3 source, (4) removal of the SiO_2 mask, (5) re-growth of SiO_2 for surface passivation, and (6) a photolithography process to open the SiO_2 layer for a contact formation within the B-BSF region. Key to success of such a complicated structure is excellent process control to diffuse B without degrading the bulk lifetime.

Despite its high complexity, this structure demonstrates the efficiency potential of Si solar cells and provides guidelines for the development of high-efficiency cells with simpler structures and processes.

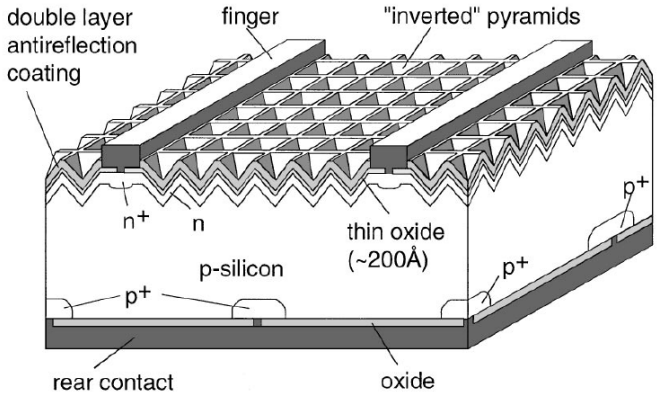


Figure 3.6 Example of a dielectric back-passivated cell structure with a LBSF: PERL cell [45].

Another structure that combines dielectric passivation with a LBSF is the laser-fired contact (LFC) solar cell developed at the Franhofer Institute [60]. The LFC structure is capable of achieving > 20% efficient cells with a photolithography front contact. A schematic of the process is shown in Figure 3.7. First, Al is deposited (either by evaporation or sputtering) on a dielectric layer. Subsequently, a spotted laser is applied to heat the Al layer locally, resulting in local openings of the dielectric layer underneath in conjunction with the formation of the LBSF by the Al-Si alloying process. The compatibility of such a process to screen-printing technology is under development [61-66].

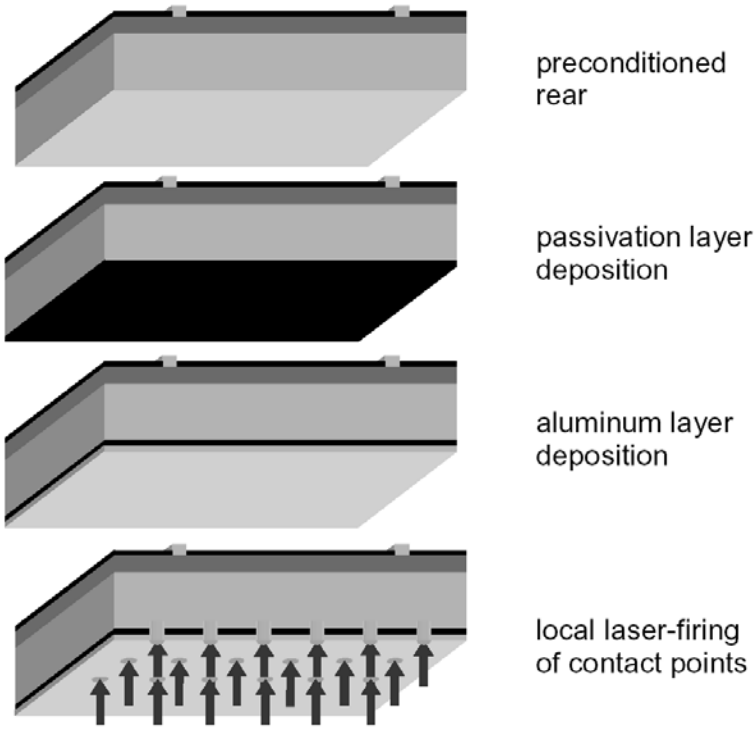


Figure 3.7 Process sequence to fabricate the LFC cell [61].

A more simplified structure involves the formation of local back contacts and a LBSF by a screen-printing process (Figure 3.8). [67]. The same concept of forming a fire-through screen-printed front contact is applied on the back side by screen-printing a metal paste dots and then firing through the dielectric layer. However, the formation of a high-quality BSF by such a method has not yet been successful.

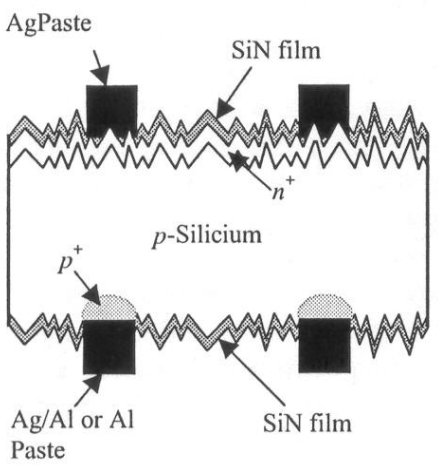


Figure 3.8 Simplified dielectric back-passivated cell by a screen-printing process [67].

3.2.3 Structure III: Dielectric Back Surface Passivation on the Floating Junction with a BSF under the Local Back Contact

Figure 3.9 shows the structure of the passivated emitter, rear floating p-n junction (PERF) cell [40]. As mentioned earlier, maintaining an electrical isolation between the floating junction and the back contact is crucial for such a structure. In the PERF cell, a B-BSF was employed around the contact area to minimize the contact recombination and to prevent the back contact shunting of the floating junction. Furthermore, an introduction of a gap between the floating junction and the B-BSF was also suggested to help reduce the recombination and any parasitic shunting at the floating junction-BSF interface (Figure 3.9) [68]. However, this resulted in a highly complicated process with several masking steps.

A dielectric layer with a high amount of positive charge (such as PECVD SiN_x) also forms a floating junction by forming an inversion layer at the surface of p-type Si. Therefore, the same consideration of maintaining an electrical isolation between the floating junction and the back contact also applies in the case of the high positively charge back dielectric.

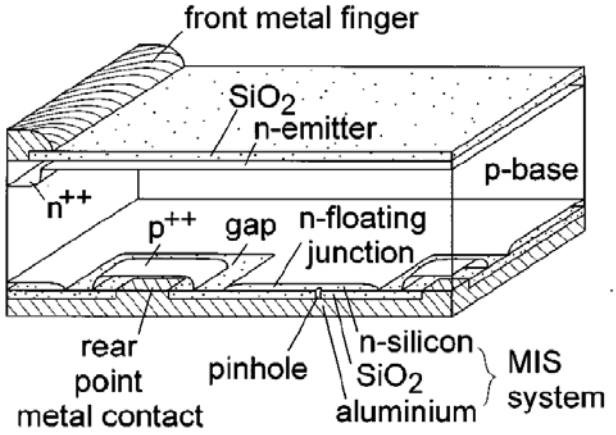


Figure 3.9 Example of a dielectric on floating-junction back-passivated cell structure with a LBSF: PERF cell [68].

3.2.4 Structure IV: Dielectric Back Surface Passivation on a Full-Area BSF with Local Back Contacts

Figure 3.10 shows the structure of the passivated emitter, rear totally diffused (PERT) cell [45, 69]. Here, the B-BSF is diffused on the entire back surface, followed by dielectric surface passivation. It has several advantages over Structure II, including reduction of lateral bulk resistance and relaxation on the quality of dielectric passivation. The necessity of forming a LBSF is also relaxed in this structure because of the full-area B-BSF. The problem associated with the fabrication of such a structure lies in the process control to diffuse B without degrading the bulk minority-carrier lifetime.

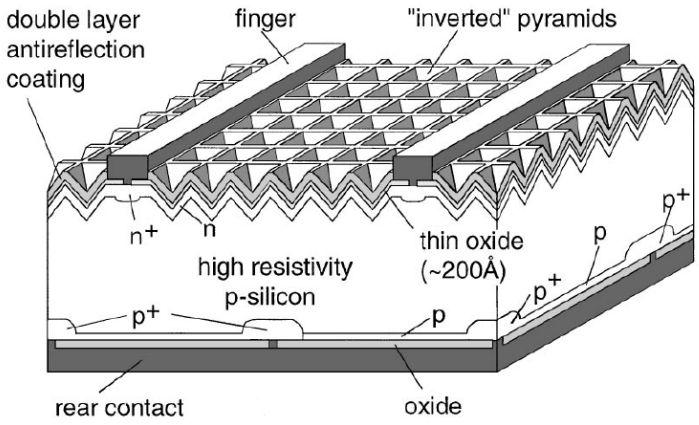


Figure 3.10 Example of a dielectric on full-area BSF back-passivated cell structure with local back contacts: PERT cell [45].

CHAPTER 4

REVIEW OF THE LIGHT INDUCED DEGRADATION IN B-DOPED CZOCHRALSKI SI SOLAR CELLS

Single crystal growth of Si using the Cz method has been steadily improved in the past two decades because of the rapid growth of semiconductor technology. The Cz method is the first choice for growing single crystal Si because it provides the ability to grow dislocation-free Si ingots with a larger diameter and a lower cost compared to ones grown by the float zone (FZ) method. However, it was found in 1973 that solar cells fabricated on p-type Si grown using the Cz method suffered from performance degradation under illumination or LID [70]. This chapter provides the understanding and literature review of the LID, which is very important because ~35% of the current solar cells are made from Cz Si. The chapter is divided into two main sections: (1) an understanding of the characteristics of the defect responsible for the LID and its origin and (2) strategies to eliminate or minimize the LID in Cz Si solar cells.

4.1 Understanding of the Characteristics of the Defect Responsible for the LID and Its Origin

Fischer and Pschunder were the first to report on the LID in Cz Si solar cells [70]. They found that the performance of Cz Si solar cells made on low resistivity (1 ohm-cm) B-doped Cz Si degraded during the first few hours of illumination (Figure 4.1a). Virtually no degradation was found in high resistivity 10 ohm-cm B-doped Cz Si or 1 and 10 ohm-cm B-doped FZ Si solar cells. This degradation occurred only in the long-wavelength response of the cells (Figure 4.1b), suggesting that the degradation is a result

of the decrease in the bulk carrier lifetime. Interestingly, the degradation was found to be reversible by a 200°C anneal in dark. No detail on the defect composition was given at that time.

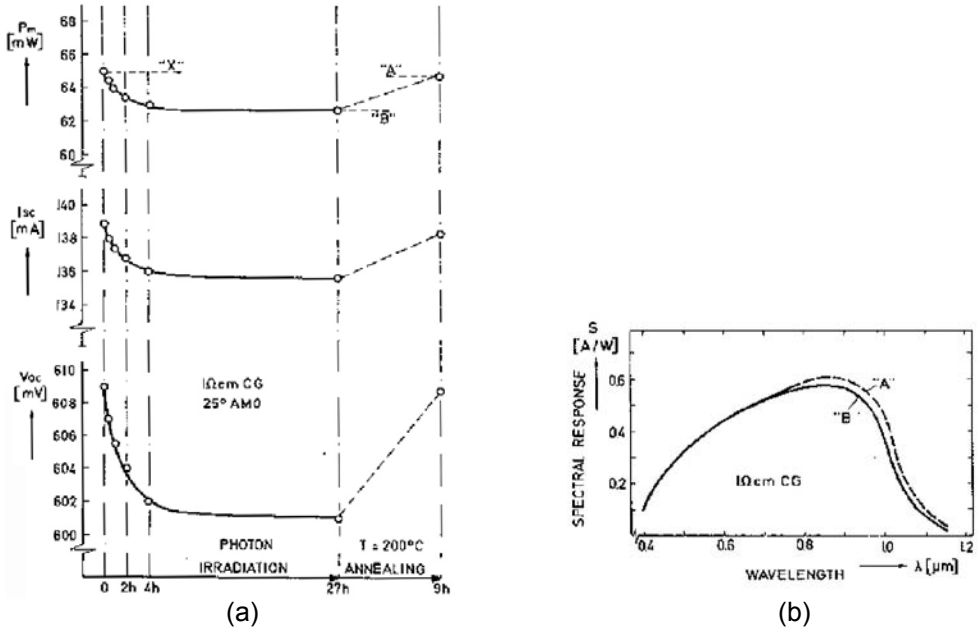


Figure 4.1 Observations of the LID in a 1 ohm-cm B-doped Cz Si solar cell: (a) the degradation and recovery cycle as a function of time and (b) the spectral response before and after the degradation [70].

Since the discovery of the LID in Cz Si solar cells, several attempts have been made to identify the defect composition and its formation mechanism. Weizer et al. proposed that the LID is caused by a metastable defect, which is a complex of a lattice defect and a single Ag atom or a cluster of Ag atoms [71]. Later, Corbett et al. suggested that the defects are not directly formed by photons, but instead by photon-induced dissociation of defect pairs [72]. Later, Reiss et al. proposed that Fe-B pair defects are responsible for the LID [73]. However, the annealing-induced recovery behavior in the work of Reiss et al. was not quite consistent with the behavior observed by Fischer and Pschunder.

Identifying the structure and the composition of the LID defect triggered the need for a quantitative analysis of the LID-defect concentration. The analysis is commonly done through minority-carrier lifetime measurements. The lifetimes of both recovered state (initial or after anneal, τ_0) and degraded state (light-soaked, τ_d) are measured. The metastable-defect concentration is then assumed to be proportional to the difference between the inverse of the degraded-state lifetime and the inverse of the recovered-state lifetime ($1/\tau_d$-$1/\tau_0$). This quantity is normally referred to as a normalized (metastable-) defect concentration (N_t^*):

$$N_t^* = \frac{1}{\tau_d} - \frac{1}{\tau_0} \qquad \text{(1/s)}. \qquad (4.1)$$

In 1997, Schmidt et al. presented a model where an interstitial B-interstitial O pair (B_i-O_i) was proposed as the core structure of the LID defect [74]. In their work, it was demonstrated that the degradation occurred only in Cz Si that was doped with B; no degradation was observed when either Ga or P was used as a dopant (Figure 4.2). Additionally, they confirmed the observation in [70] that a high resistivity 10 ohm-cm B-doped Cz Si cell exhibited virtually no degradation. These results suggested that B participates in the defect formation. The B_i-O_i pair was then suggested as the source of the LID defect by Schmidt et al. because they found that the recovery-annealing characteristic of the LID defects was similar to that of the B_i-O_i defects reported in the literature [75]. Schmidt et al. also observed a linear relationship between the normalized defect concentration and the product of the B concentration and the O_i concentration (Figure 4.3). Including O_i as a component of the LID defect supports the observation in [70], where cells made on FZ Si, which typically contains a small or negligible amount of O_i, did not suffer from the LID.

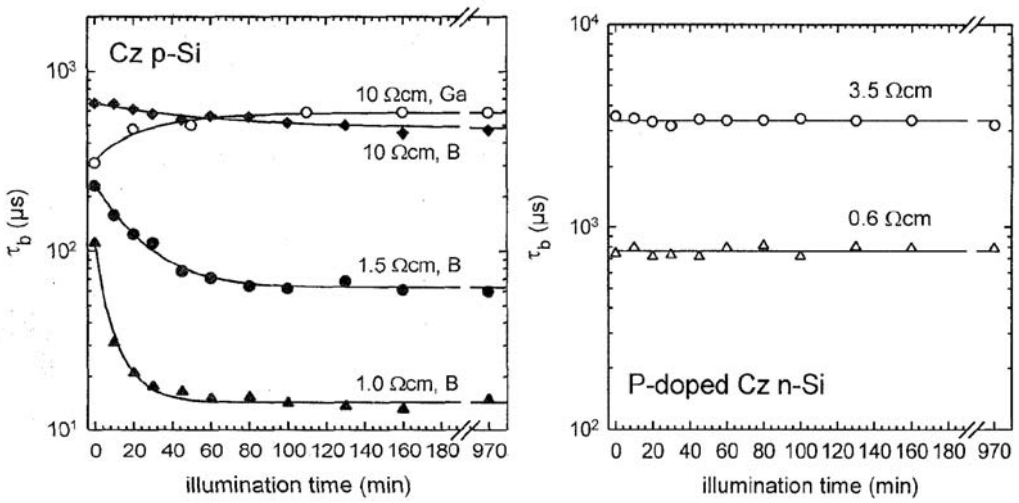


Figure 4.2 Minority-carrier lifetimes of Cz Si materials with different doping concentrations of (a) B or Ga and (b) P [74].

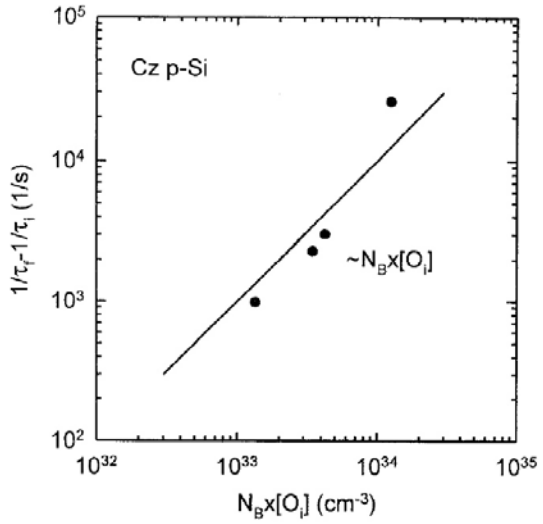


Figure 4.3 Normalized metastable-defect concentration as a function of the product of the B-doping concentration and the O_i concentration in Cz Si materials [74].

In 2001, the experimental results by Rein et al. revealed that the defect-generation rate exhibited a quadratic relationship to the doping concentration and was only weakly dependent on the injection level (see Figure 4.4). Additionally, they found the activation energy of the defect-annihilation rate to be 1.32±0.05 eV (see Figure 4.5).

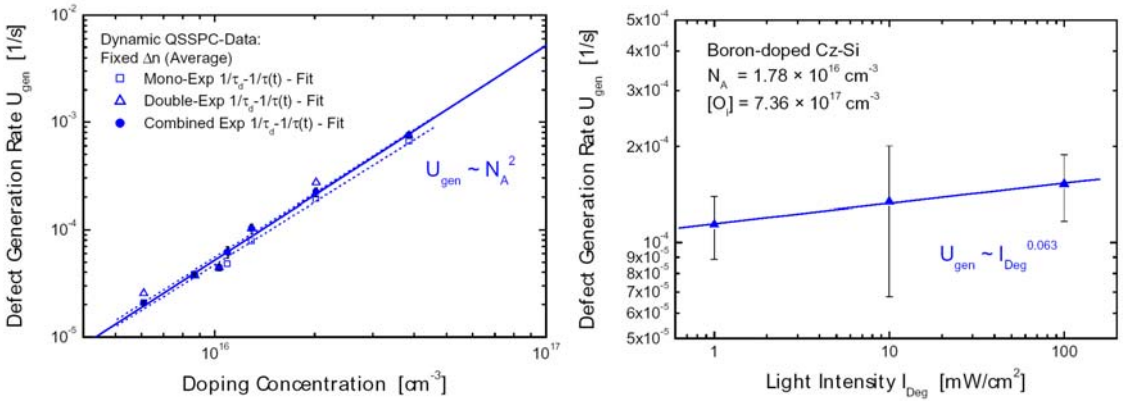


Figure 4.4 LID-defect generation rate as a function of the B doping concentration and the light intensity [76].

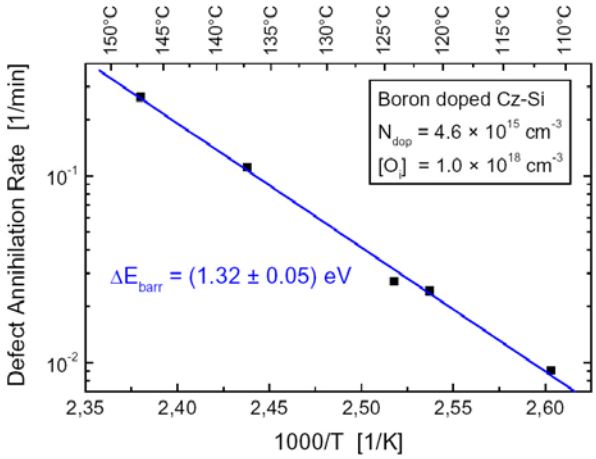


Figure 4.5 Arhenious plot of the annihilation rate of the LID defects showing an activation energy of 1.32±0.05 eV [76].

Hashigami et al. also found that the LID-defect generation rate was independent of the light intensity at intensity above 1 mW/cm^2 but became a function of the light intensity at intensity below 1 mW/cm^2 [77]. Hashigami et al. also pointed out on rapid degradation at the onset of the LID.

In 2002, Schmidt et al. proposed that the LID defect is composed of one B_s atom and two O_i atoms (O_i dimer or O_{2i}) [78]. They proposed that the generation of the LID defect is governed by the diffusion or the migration of an O_i dimer, which has a much higher

diffusion coefficient compared to a single O_i at a room temperature in the Si lattice. Their model is represented by the schematic shown in Figure 4.6 and is based on the following experimental observations:

- The defect generation is thermally activated (Figure 4.7).
- The activation energy of the defect generation is 0.4 eV, which lies in the energy range of the migration energy of O_{2i} reported in the literature [79].
- The defect concentration exhibits a quadratic relationship to the O_i concentration (Figure 4.8).

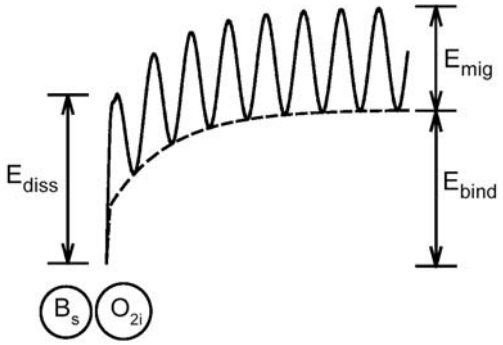


Figure 4.6 Model for the LID-defect generation and annihilation proposed in [78]. E_{diss} is the dissociation energy of the B_s-O_{2i} complex (or the activation energy of the LID-defect annihilation process), E_{mig} is the migration energy of the O_i dimmer (or the activation energy of the LID-defect generation process), and E_{bind} is the binding energy of the B_s-O_{2i} complex.

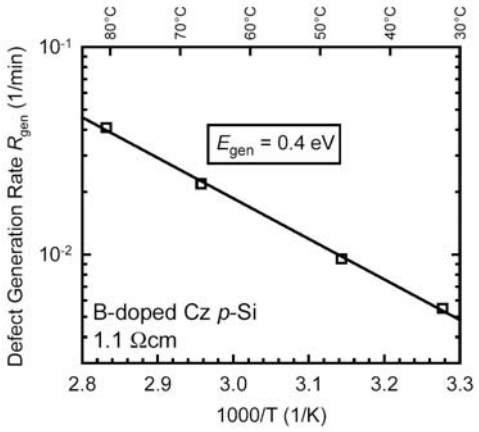


Figure 4.7 Arhenious plot of the generation rate of the LID defects showing an activation energy of 0.4 eV [78].

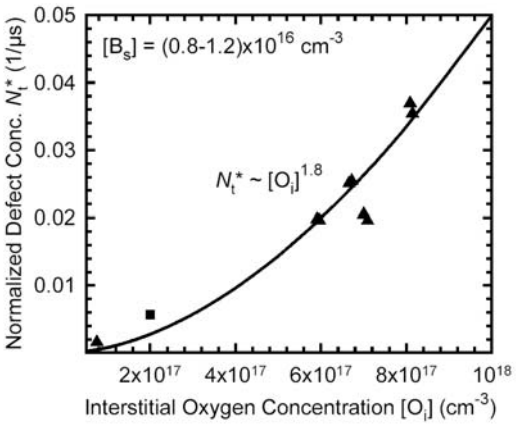


Figure 4.8 Relationship between the LID-defect concentration and the O_i concentration [78]. A quadratic relationship was observed.

In 2003, Rein and Glunz applied temperature dependent lifetime spectroscopy (TDLS) and injection level dependent lifetime spectroscopy (IDLS) to obtain more information about the electronic configuration of the LID defects (see Figure 4.9) [80]. They established that the electron capture cross-section of the LID defect is an inversed quadratic function of the temperature ($\sigma_n = \sigma_{n0} \times T^{-2}$), which suggested that the LID defect is an attractive-coulombic type center. Rein and Glunz further established the ratio of the electron-to-hole capture cross section (σ_n/σ_p) of the LID defect to be ~9. Finally, they proposed that the defect level lies at E_c-0.41 eV.

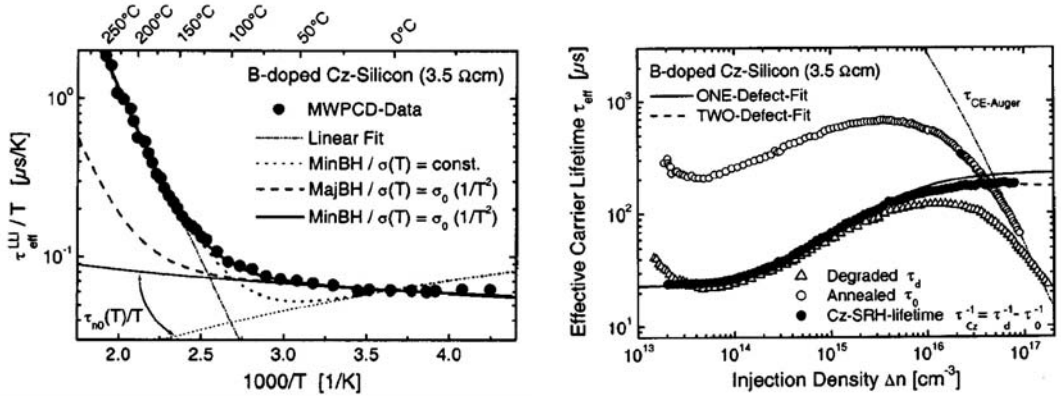


Figure 4.9 Analyses to obtain the information of the electronic configuration of the LID defects [80]: (a) TDLS and (b) IDLS.

In 2004, Schmidt published two comprehensive reviews on the LID [81, 82], which summarizes many of the findings above.

In 2006, Bothe and Schmidt gave a detailed understanding of both fast- (rapid degradation at the beginning of the degradation period as observed by Hashigami in [77]) and slow-forming LID defects [83].

Also in 2006, Herguth et al. [84, 85] reported that prolonged carrier injection (either by illumination or electrical bias) at an elevated temperature (>70°C) could recover the LID-degraded cell performance (see Figure 4.10). They attributed this recovery process to transformation of the degraded state to a new state called "regenerated state" (see Figure 4.11), which is relatively inactive in terms of recombination. This regenerated state was found to be stable under a normal solar cell operating condition, but was found to be unstable when the sample was heated to >200°C in the dark. They proposed that the anneal above 200°C converted the regenerated state back to the annealed (or non-degraded) state, which then could be transformed into the degraded state by carrier injection. Finally, they found the activation energy of the regeneration process to be 0.62 eV (see Figure 4.12).

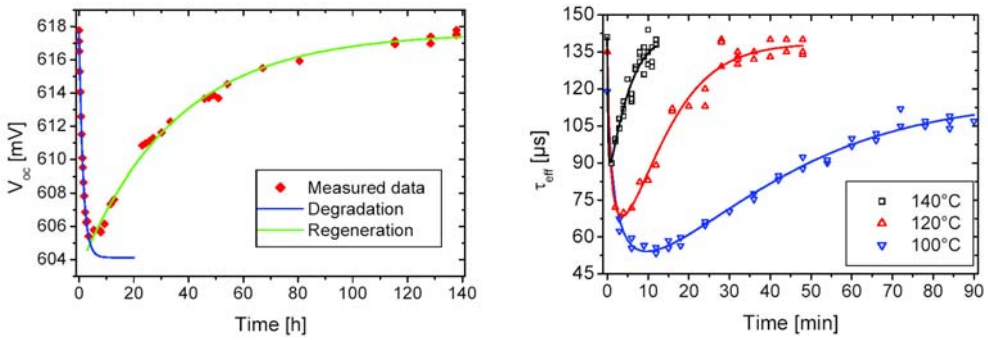


Figure 4.10 Observation of the recovery (regeneration) from the LID by prolonged carrier injection at an elevated temperature: (a) V_{oc} of the B-doped Cz Si cell (regenerated at 70°C under illumination) and (b) effective lifetime on the B-doped Cz Si samples (regenerated at 100, 120, and 140°C under illumination) [85].

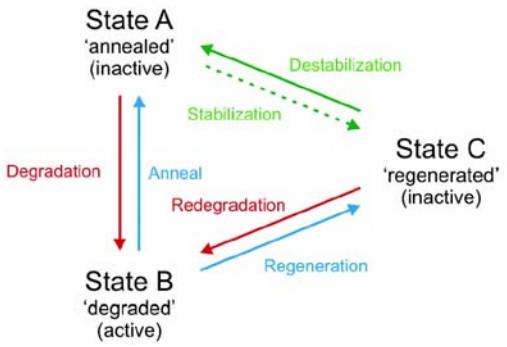


Figure 4.11 Schematic representation of the three LID-related defect states proposed in [85]: (a) annealed state, (b) degraded state, and (c) regenerated state.

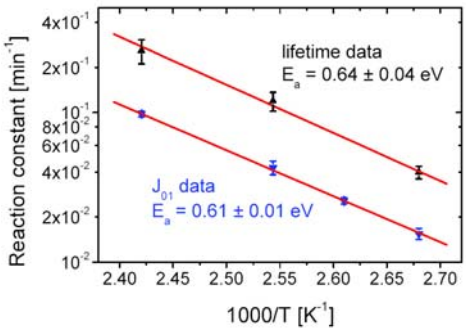


Figure 4.12 Arhenious plot of the regeneration of the LID defects showing an activation energy of ~0.62 eV [85].

The important findings on the characteristic of the LID discussed in this section are summarized in Table 4-1.

Table 4-1 Summarized important findings on the characteristic of the LID in B-doped Cz Si.

Year	Author(s) [reference]	Experimental observations	Proposed defect composition	Defect-generation mechanism
1973	Fischer and Pschunder [70]	- First observation of the LID in B-doped Cz Si solar cells - Recovery anneal of ~200°C in the dark - Degradation caused by the degradation in the bulk lifetime - No LID in FZ Si and high ρ B-doped Cz Si	N/A	Photon-induced
1979	Weizer et al. [71]	Degradation caused by a forward bias as well	A complex of a lattice defect and a single Ag atom or a cluster of Ag atoms	Minority-carrier injection induced change in the charge state of passive defects
1980	Corbett et al. [72]	N/A	Defect pair	Dissociation of defect pairs by photons
1996	Reiss et al. [73]	N/A	Fe-B	Dissociation of Fe-B pairs by photons, minority-carrier injection, or a thermal treatment
1997	Schmidt et al. [74]	- No LID in Ga- or P-doped Cz Si - $N_t \propto [B_S] \times [O_i]$	B_i-O_i	Dissociation of B_i-C_s pairs by photons followed by pairing of B_i and O_i
2001	Rein et al. [76]	- $R_{gen} \propto [B_S]^2$ - Weak dependency of R_{gen} on the intensity for intensity > 1 mW/cm^2 - Activation energy of the defect annihilation (E_{ann}) ~1.32 eV	N/A	N/A
2001	Hashigami et al. [77]	- Intensity dependency of R_{gen} for intensity <1 mW/cm^2 - Intensity independency of R_{gen} for intensity > 1 mW/cm^2 - Observation of rapid degradation in the initial regime of the degradation	N/A	N/A
2002	Schmidt et al. [78]	- Temperature dependency of R_{gen} - Activation energy of the defect generation (E_{gen}) ~0.4 eV - $N_t \propto [O_i]^2$	B_S-O_{2i}	Fast diffusing O_{2i} captured by B_s to form B_s-O_{2i}
2003	Rein and Glunz [80]	- $\sigma_n=\sigma_{n0} \times (T^{-2})$ (attractive coulombic type center) - $\sigma_n / \sigma_p = 9.3$ - $E_t=E_c$-0.41 eV	N/A	N/A
2006	Herguth et al. [84, 85]	- The LID can be recovered by prolonged carrier injection at an elevated temperature (>70°C) - The recovered state is stable at least under a normal solar cell operation	N/A	N/A

4.2 Strategies to Eliminate or Minimize the LID

As discussed in the previous section, B and O were established as being responsible for the LID in B-doped Cz Si solar cells. The LID is most pronounced in regular p-type Cz Si solar cells because they typically exhibit a high initial carrier lifetime (dislocation-free property), contain B as a p-type dopant, and contain a high O_i concentration (because silica is generally used as a crucible). In practice, the LID can be avoided by (1) eliminating the use of B doping or reducing the B-doping concentration, (2) eliminating or minimizing the incorporation of O_i during the crystal growth, and (3) developing solar cell processing steps to manipulate the O_i concentration. Apart from the above strategies, the finding by Herguth et al. showed that the LID could also be overcome by (4) converting the LID-degraded states to regenerated states that are relatively inactive in terms of recombination. These four strategies are reviewed in detail below.

4.2.1 Eliminating or Minimizing the Use of B Doping

There are three main strategies to eliminate or to minimize the use of B-doping in Cz Si:

(a) Use of high resistivity B-doped Cz

(b) Use of n-type dopants such as P

(c) Use of alternative p-type dopants such as Al, Ga, or In

As mentioned in the previous section, high resistivity (10 ohm-cm) B-doped Cz Si was found to exhibit no LID. Glunz et al. also showed that the LID could be avoided (Figure 4.13) by reducing the B-doping concentration below 2×10^{15} cm^{-3} (i.e., resistivity of higher than 7 ohm-cm) [86, 87].

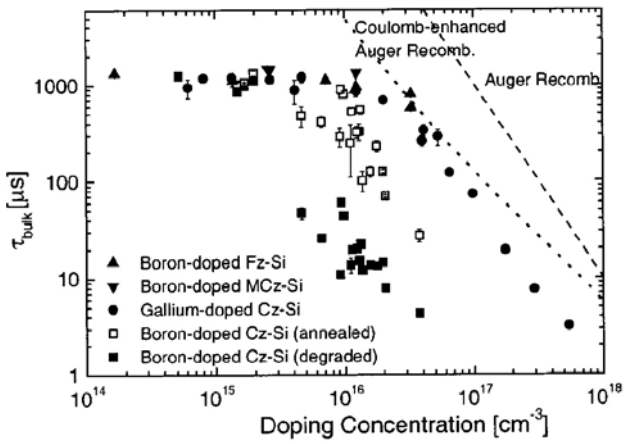


Figure 4.13 Measured minority-carrier lifetimes in different single crystalline Si materials as a function of doping concentrations of B and Ga dopants [87].

Doping Cz Si with P or Ga was found to give a high lifetime and no LID [74, 88-92] (see also Figure 4.2). However, other dopants, such as Al and In, showed somewhat inferior minority-carrier lifetime, even in FZ Si [93].

The use of Ga as a p-type dopant has an advantage over using P as an n-type dopant because Ga provides complete elimination of the LID without the need to modify the cell structure or the processing equipment. Nevertheless, there are some drawbacks associated with the use of Ga. First, use of a Ga dopant gives rise to complication of managing the Si feedstock [94]. Most Cz Si manufacturers for a solar cell application rely on externally supplied remelt or potscrap. As Ga-doped remelt is not available on the open market, this situation likely necessitates the recycling of internally produced remelt, subsidized with virgin Si. Relying on virgin suppliers is not a cost-effective option and creates a significant risk since the availability and, more importantly, the cost of virgin Si fluctuates greatly. The other drawback of using Ga as a dopant is the low segregation coefficient of Ga in Si (k=0.008) (compared to k=0.8 of B in Si) [95]. This results in a much wider variation in the resistivity along Ga-doped ingots. For example, for an ingot

length of ~0.90-0.95 m with target resistivity of 1 ohm-cm, the resistivity of a Ga-doped ingot varies from 0.57 to 2.54 ohm-cm, while the resistivity of a B-doped ingot varies from 0.87 to 1.22 ohm-cm.

Many attempts have been made to investigate the effect of the resistivity variation on solar cell performance. Glunz et al. fabricated solar cells on Ga-doped wafers with three resistivity values of 3.4, 5.2 and 22 ohm-cm using the random-pyramid PERL structure and were able to achieve cell efficiency in a relatively tight range of 20.8 to 21.4% (see Figure 4.14) [88].

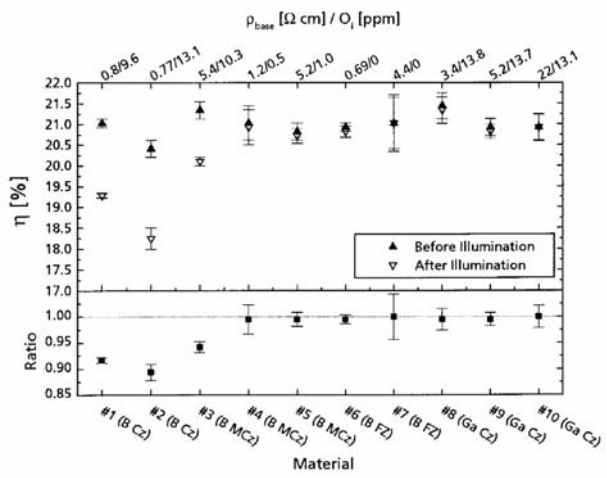


Figure 4.14 Efficiency of PERL-type solar cells fabricated on different Cz Si materials before and after illumination [88].

Metz et al. applied the obliquely evaporated contact (OECO) process on Ga-doped samples with lower resistivity in the range of 0.08 to 1.34 ohm-cm. They found a suitable range of the resistivity for achieving high-efficiency cells to be from 0.25 to 1.34 ohm-cm, below which, the efficiency dropped rapidly (see Figure 4.15) [90]. Metz et al. attributed the drop in the efficiency at low resistivity to the low bulk lifetime (<80 μs) as a result of Auger recombination at higher doping concentrations.

A similar resistivity range of 0.05 to 1.5 ohm-cm was investigated by Glunz et al. using the random-pyramid PERC structure [96]. They also observed a drop in the efficiency (Figure 4.16) when the resistivity fell below 0.2 ohm-cm (doping concentration above 1×10^{17} cm^{-3}). Glunz et al. attributed the drop in the efficiency at high-doping concentrations to (1) low bulk lifetime and (2) band gap narrowing effect on the base side of the p-n junction, which reduces the V_{oc} of the cells.

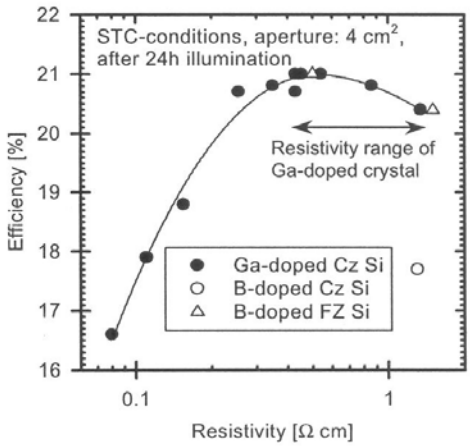


Figure 4.15 Efficiency of OECO-type solar cells as a function of doping concentrations for Ga-doped Cz Si, B-doped Cz Si, and B-doped FZ Si after illumination [90].

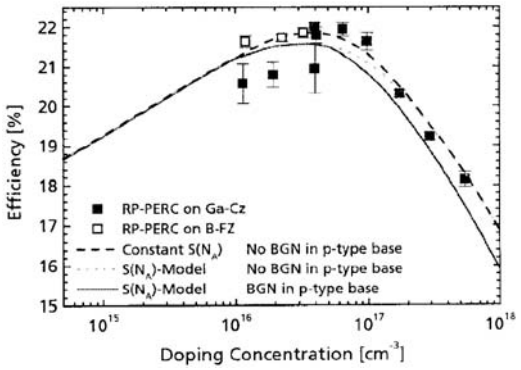


Figure 4.16 Efficiency of random-pyramid PERC type solar cells as a function of doping concentrations for Ga-doped Cz Si and B-doped FZ Si cells [96].

Note that the solar cell structures used in all these studies utilized thermally grown SiO_2 as a passivation layer. The fabrication of these cells, therefore, involved a high temperature oxidation step.

4.2.2 Eliminating or Minimizing the Incorporation of O During the Crystal Growth

There are two main strategies to eliminate or to minimize the incorporation of O into single crystalline Si wafers:

(a) Avoiding the use of a silica crucible by the use of FZ method (crucible-free)

(b) Minimizing the incorporation of O into the Si melt during the Cz Si growth by the use of magnetic field (MCz). Here, according to Lenz's law, a magnetic field is used to retard the flow of the Si molten, which is highly electrically conductive at high temperatures, in the crucible. This minimizes the incorporation of O from the crucible to the ingot through melt convection

As discussed in Section 4.1, FZ Si, which normally contains a low or negligible amount of O_i, does not exhibit any LID. Nevertheless, FZ Si is typically more expensive than regular Cz Si (up to five times).

Glunz et al. demonstrated that B-doped MCz Si with a low O_i concentration could be used to fabricate LID-free solar cells [88] (see also Figure 4.14). Zhao et al. was also able to achieve an efficiency of 24.5% on low-O_i MCz Si using the PERT structure and found the cell performance to be stable at least after one day under one-sun illumination [45]. Additionally, Saitoh et al confirmed through a bulk carrier lifetime analysis that low O_i MCz Si did not exhibit any LID [97].

4.2.3 Developing Solar Cell Processing Steps to Manipulate the O_i Concentration

Many different heat treatments that offer permanent reduction of the LID have been proposed in the literature. Glunz et al. demonstrated that an oxidation at 1,050°C with an appropriate ramp-up rate could enhance the stable carrier lifetime in B-doped Cz Si by a factor of 2 to 3 (see also Figure 4.17) [86]. They found that the holding time was not critical for the LID reduction. Another investigation by Rein et al. confirmed the effectiveness of the 1,050°C oxidation (with a proper ramp-up rate) for the LID reduction [98] (Figure 4.18). Interestingly, they also observed a similar amount of the reduction of the LID by a much lower oxidation temperature of 750°C. Rein et al. suggested that the optimum ramp-up rate corresponded to the one that resulted in a moderate reduction of the O_i concentration (Figure 4.19). They found that an improper ramp-up rate gave a lower O_i concentration but also a lower stable bulk lifetime, which they attributed to the formation of O-precipitation defects.

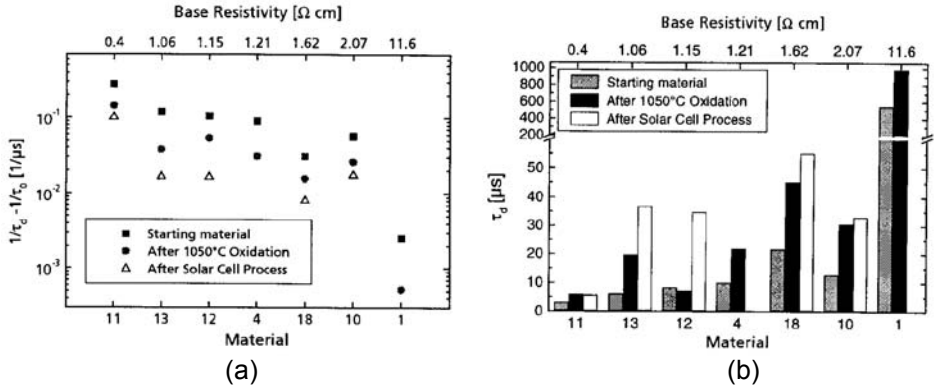


Figure 4.17 Effect of an oxidation process at 1,050°C with a proper ramp-up rate on B-doped Cz Si materials in terms of (a) the normalized metastable-defect concentration and (b) the stable bulk minority-carrier lifetime [86].

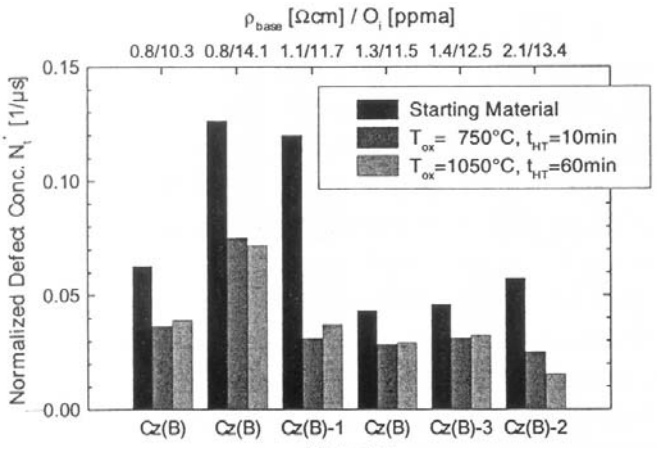


Figure 4.18 Comparison of the reduction of the normalized matastable defect concentration by an oxidation process at 750°C for 10 minutes or at 1,050°C for 60 minutes for different B-doped Cz Si materials [98].

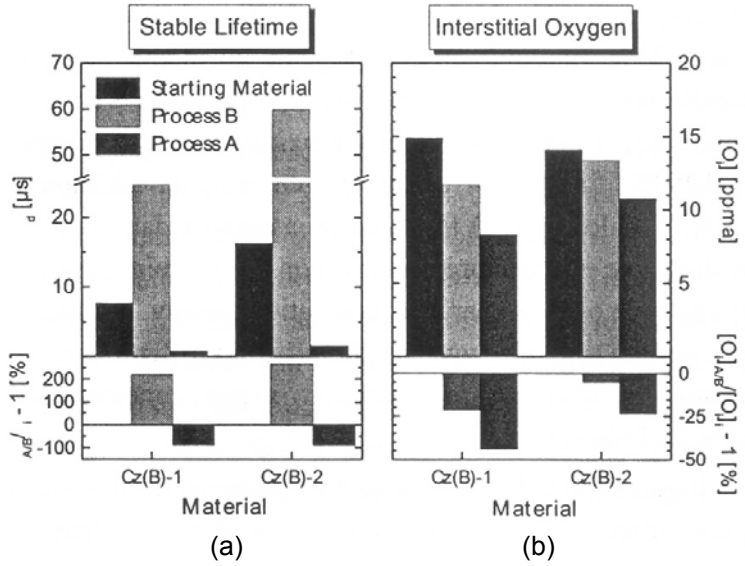


Figure 4.19 Effect of different process schemes (A and B) on (a) the stable (light-soaked) minority-carrier lifetime and (b) the O_i concentration in B-doped Cz Si materials [98]. Both Processes A and B included an oxidation process at 1,050°C for 30 minutes (in O with an addition of Dichloroethylene) followed by a post-oxidation anneal at the same temperature in Ar ambient for 30 minutes. The only difference between the two processes was the ramping condition: Process A had unsuitable ramping and Process B had the optimized ramping.

Bothe et al. demonstrated that an anneal at 850°C, regardless of whether the ambient is O_2 or N_2, could reduce the LID-defect concentration by up to a factor of 3.5 (Figure 4.20) [99]. They also found that the holding time was not a critical parameter for the LID

reduction. Additionally, a faster ramp-down rate was found to be more effective in reducing the LID defects.

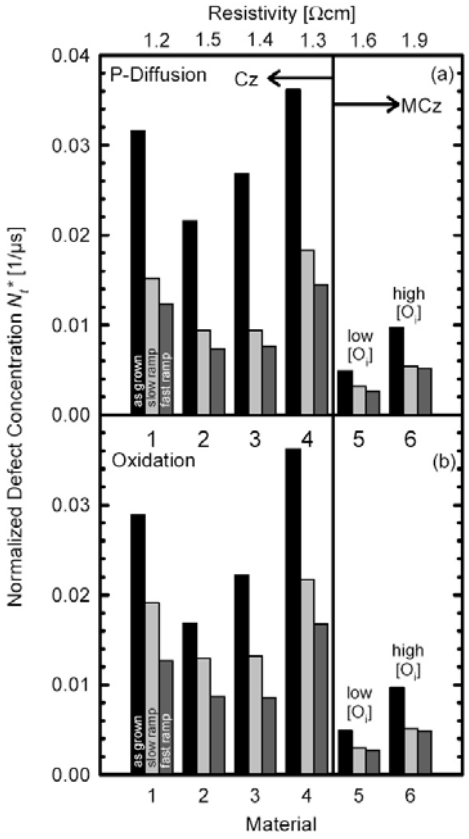


Figure 4.20 Reduction of the LID defects in Cz Si materials by phosphorus diffusion or oxidation at 850°C. Similar results between the two suggested that the thermal treatment is responsible for the improvement, not the phosphorus gettering [99].

Several short time annealing schemes for the LID reduction were also reported in the literature. Nagel et al. demonstrated that an anneal in a belt furnace at 820°C for a short dwelling time of 8 s could reduce the LID defects by a factor of 1.4 to 2.4 (Figure 4.21) [100]. Lee et al. investigated rapid thermal annealing and found the optimum annealing condition for the LID reduction to be 900°C for 2 minutes (Figure 4.22) [101].

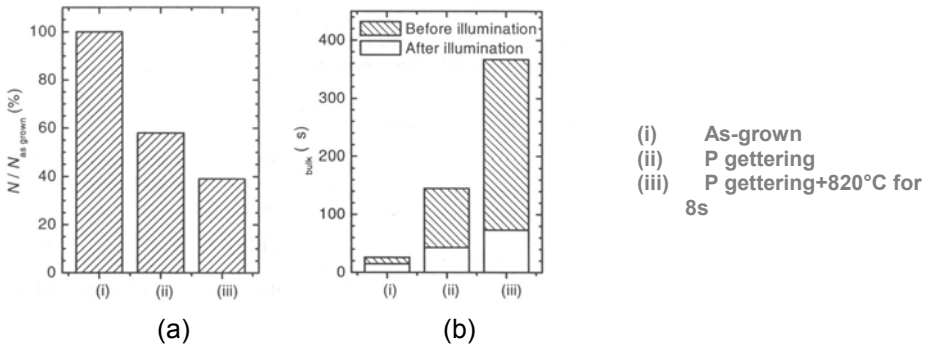


Figure 4.21 Effect of P-gettering and a subsequent anneal at 820°C for 8 s in a belt furnace on B-doped Cz Si materials in terms of (a) the metastable-defect concentration normalized to the as-grown state and (b) the bulk minority-carrier lifetime before and after illumination [100].

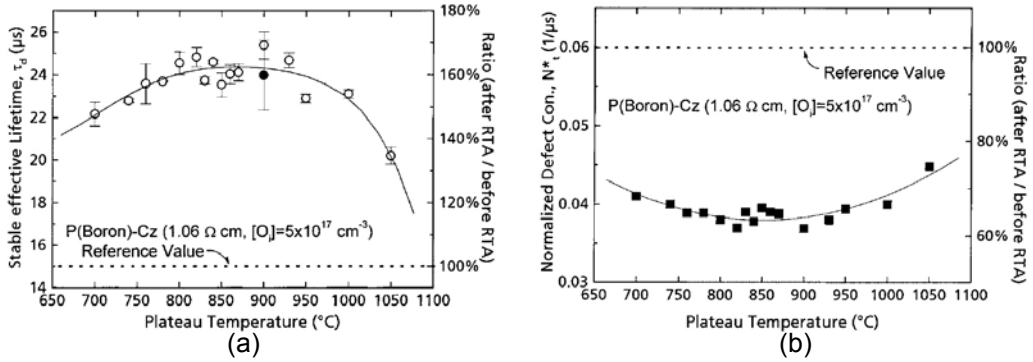


Figure 4.22 Effect of a rapid thermal anneal as a function of peak temperatures on B-doped Cz Si materials in terms of (a) the stable effective lifetime and (b) the normalized metastable-defect concentration [101]. The annealing time was fixed at two minutes for all cases. The stable effective lifetime corresponded to a light-soaked lifetime measured with SiN_x as a passivation layer.

Hydrogenation of defects was also proven to be very effective for the LID reduction. Schmidt et al. demonstrated that a hydrogenation process could reduce the LID defects by a factor of 2 to 3.5. This was done by a deposition of a PECVD SiN_x layer, which contained a large amount of H, followed by an anneal at 750°C for 60 seconds (Figure 4.23) [102]. The same annealing without the SiN_x layer did not result in any reduction of the LID defects.

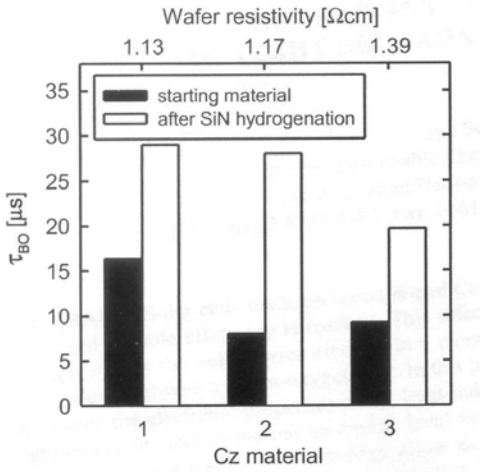


Figure 4.23 Effect of hydrogenation on the metastable-defect lifetime (an inverse of the normalized metastable-defect concentration) in B-doped Cz Si materials [102].

Based on the defect-formation mechanism proposed by Schmidt et al in [78], Bothe et al. demonstrated that the LID defects could be reduced by a prolonged anneal at 450°C (Figure 4.24) [99]. They attributed the benefit of such annealing to the formation of other types of thermal donor that consumed and reduced O_{2i} in the Si bulk. A reduction of the LID defects by up to a factor of 3.3 was demonstrated using this technique.

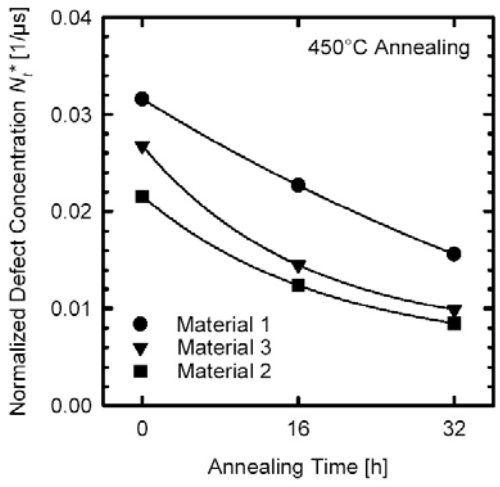


Figure 4.24 Reduction of the LID defects in B-doped Cz Si materials by a prolonged anneal at 450°C [99].

Schmidt et al. proposed in [103] that the LID could also be alleviated by using C-rich Si. C is expected to form C_s-O_{2i} such that less O_{2i} is available for the LID-defect formation. The LID reduction by 30% was demonstrated using such a technique [82].

4.2.4 Converting LID Degraded States to Stable Inactive (Regenerated) States

Another technique to overcome the effect of the LID was proposed by Herguth et al [84, 85], where they demonstrated that prolonged carrier injection (either by illumination or electrical bias) at an elevated temperature (>70°C) could recover the performance of the LID-degraded B-doped Cz Si solar cell back to virtually the same level as the non-degraded state (Figure 4.25).

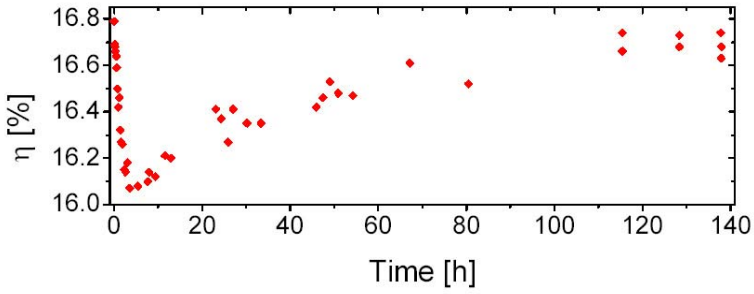


Figure 4.25 The recovery (regeneration) of the efficiency of an LID-degraded B-doped Cz Si cell by prolonged illumination at 70°C [85].

This new strategy to overcome the LID is very promising because virtually full recovery can be achieved at a relatively low annealing temperature. Nevertheless, the technique requires prolonged annealing, which could hinder its direct application.

The strategies to avoid or alleviate the LID that are discussed in this section are summarized in Table 4-2.

Table 4-2 Summarized strategies to avoid or alleviate the LID in B-doped Cz Si.

General idea	Specific strategy	Degree of the LID reduction	Pro	Con
Eliminating the use of B doping or reducing the B doping	Use of high ρ B-doped Cz Si	Complete elimination for ρ >7 ohm-cm	No change in the solar cell structure and the dopant	- Series resistance - Need of excellent back surface passivation
	Use of P-doped Cz Si	Complete elimination	Generally higher minority-carrier lifetime than a p-type material	Complete change of the solar cell structure
	Use of Ga-doped Cz Si	Complete elimination	No change in the solar cell structure	- Silicon feedstock management - Resistivity variation along the ingot
Eliminating or minimizing the incorporation of O during the crystal growth	Use of FZ Si	Complete elimination	Generally higher minority-carrier lifetime than Cz Si	More expensive than Cz Si
	Use of MCz Si	Complete elimination for low O_i	No change in the solar cell structure and the dopant	Additional cost for installing and operating magnetic unit for the Si growth
Manipulating the O_i concentration	750°C or 1,050°C oxidation with a proper ramp-up rate	Improve τ_{stable} by a factor of 2-3	No change in the solar cell structure and the dopant	- Not a complete elimination of the LID - Need of an oxidation step
	850°C anneal (in N_2 or O_2 ambient)	Reduction of N_t by up to a factor of 3.5	No change in the solar cell structure and the dopant	- Not a complete elimination of the LID - Need of an anneal in a tube furnace
	Belt anneal at 820°C for 8 s	Reduction of N_t by a factor of 1.4 to 2.4	- No change in the solar cell structure and the dopant - Short time anneal with compatibility to a screen-printing process	Not a complete elimination of the LID
	RTP anneal at 900°C for 2 minutes	Improve τ_{stable} by up to a factor of 1.7	- No change in the solar cell structure and the dopant - Short time anneal	- Not a complete elimination of the LID - Additional process step (the anneal is likely too aggressive for a screen-printing process)

Table 4-2 continued.

Manipulating the O_i concentration	Hydrogenation by a deposition of PECVD SiN followed by a short-time anneal	Reduction of N_t by a factor of 2 to 3.5	- No change in the solar cell structure and the dopant - Short time anneal with compatibility to a screen-printing process	Not a complete elimination of the LID
	Long time anneal at 450°C (up to 32 hrs)	Reduction of N_t by up to a factor of 3.3	- No change in the solar cell structure and the dopant - Anneal at a relatively low temperature	- Not a complete elimination of the LID - Need of a prolonged anneal
	Use of C-rich Si	Reduction of N_t by 30%	No change in the solar cell structure and the dopant	- Not a complete elimination of the LID - Change in the raw material
Transformation of active defect states to stable passive defect states	Prolonged carrier injection at an elevated temperature (>70°C)	Virtually a full recovery	- No change in the solar cell structure and the dopant - A very low temperature anneal	Need of a prolonged anneal

CHAPTER 5

INVESTIGATION OF GA-DOPED CZ SI MATERIALS FOR SI SOLAR CELLS

As pointed out in Chapter 4, doping a crucible-grown Cz Si ingot with Ga offers a sure way of eliminating the LID because the LID defect is composed of B and O complex. However, the low segregation coefficient of Ga in Si causes a much wider resistivity variation along the Ga-doped Cz Si ingot. Therefore, in this study, to examine the possibility of using Ga-doped Cz Si for the PV application, both B- and Ga-doped Cz ingots were grown in an industrial environment at the Shell Solar Industries and analyzed in detail before and after processing and a light exposure. Because of the resistivity variation, the Cz Si wafers from different locations along the Ga- as well as the B-doped ingots were analyzed. Both the ingots were targeted to have nominal resistivity of 1 ohm-cm. Table 5-1 summarizes resistivity values and locations of the wafers on the ingots used in this study. To evaluate the material quality along the ingot, the bulk lifetime was determined for both ingots by the contactless photoconductance measurement [104, 105]. Additionally, manufacturable screen-printed solar cells were fabricated and analyzed using light I-V measurements.

Table 5-1 Summary of B- and Ga-doped Si samples used in the study.

Ingot	Thickness		Tail end								Seed end
B-doped	290 μm	Location	1	2	3	4	5	6			
		ρ (ohm-cm)	0.87	0.82	0.90	0.95	1.00	1.22			
Ga-doped	290 μm	Location	1	2	3	4	5	6	7	8	9
		ρ (ohm-cm)	0.57	0.63	0.84	0.99	1.19	1.46	1.82	2.17	2.54

5.1 Resistivity Distribution

Table 5-1 shows that the low-resistivity B-doped ingot provided samples with tight resistivity control, ranging from 0.87 ohm-cm to 1.22 Ω-cm. On the other hand, the resistivity variation was much larger (0.57-2.54 ohm-cm) in the case of the Ga-doped ingot. The resistivity decreased appreciably from the seed to the tail end of the Ga-doped ingot because of the low segregation coefficient of Ga in Si (k_0=0.008 for Ga compared to k_0=0.8 of B).

5.2 As-Grown and Post-Diffusion Lifetimes

The bulk minority-carrier lifetime in each sample was measured in an as-grown state and after a phosphorus diffusion step. The post-diffusion lifetime was measured on each sample after $POCl_3$ diffusion at 880°C followed by etching the sample down to Si bulk. For the as-grown and the post-diffusion lifetimes, the measurements were performed after (1) 200°C anneal to remove any LID and (2) light-soaking for >20 hours to obtain the stabilized lifetimes after the LID. The surface was passivated by an iodine/methanol solution during the lifetime measurements. All the bulk lifetime measurements were performed at an injection level of 2×10^{14} cm^{-3}.

The as-grown and the post-diffusion lifetimes for the B-doped Cz Si samples are summarized in Figure 5.1a and b, respectively. The B-doped ingot showed a very tight distribution of the lifetime except at the seed end, where the lifetime was somewhat lower probably because of the swirl defects that occur in macroscopically dislocation-free Si with a high density of point defects [106].

Figure 5.1 reveals that the phosphorus diffusion enhanced the light-soaked lifetime significantly. This is attributed to (1) impurity gettering by phosphorus diffusion [107] and (2) reduction of the LID defects through high-temperature annealing (as discussed in Chapter 4). For these reasons, the lifetime in a finished cell correlates better with the post-diffusion lifetime than the as-grown lifetime.

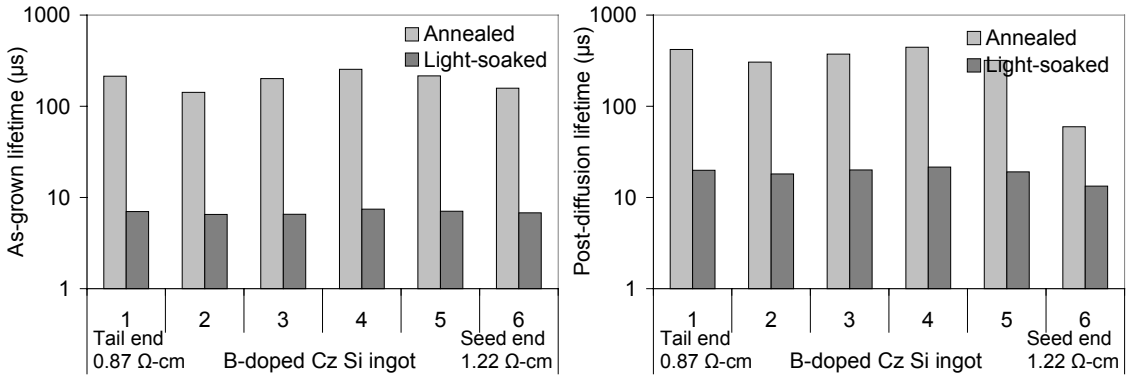


Figure 5.1 (a) As-grown and (b) post-diffusion lifetimes before and after light-soaking on wafers from different locations of the B-doped Cz ingot.

To assess the effectiveness of the high temperature process in reducing the LID defects, the metastable defect concentration (N_t^*) before and after the diffusion process are plotted side by side in Figure 5.2 (refer to Chapter 4 for the calculation of N_t^*). The data revealed that the phosphorus diffusion reduced the metastable defect concentration

by a factor of 2.8-3.1; however, the LID still managed to lower the post diffusion lifetime by a factor of 15-20, from ~300-400 μs to ~20 μs (Figure 5.1b).

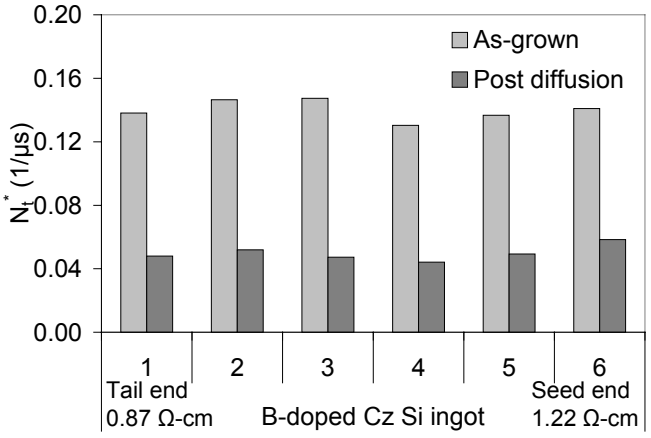


Figure 5.2 Normalized metastable defect concentration in the B-doped Cz wafers before and after a diffusion process.

The as-grown and the post-diffusion lifetimes for the Ga-doped Cz samples are summarized in Figure 5.3a and b, respectively. Unlike the B-doped samples, the Ga-doped samples did not show any LID. However, the lifetime in Ga-doped ingot varied significantly. The lifetime increased from the tail to the seed end except for a drop at the seed end because of the swirl defects, as observed in the case of the B-doped ingot. Notice that the phosphorus diffusion improved the lifetime of the Ga-doped Cz wafers by a factor of ~1.3 because of gettering of impurities.

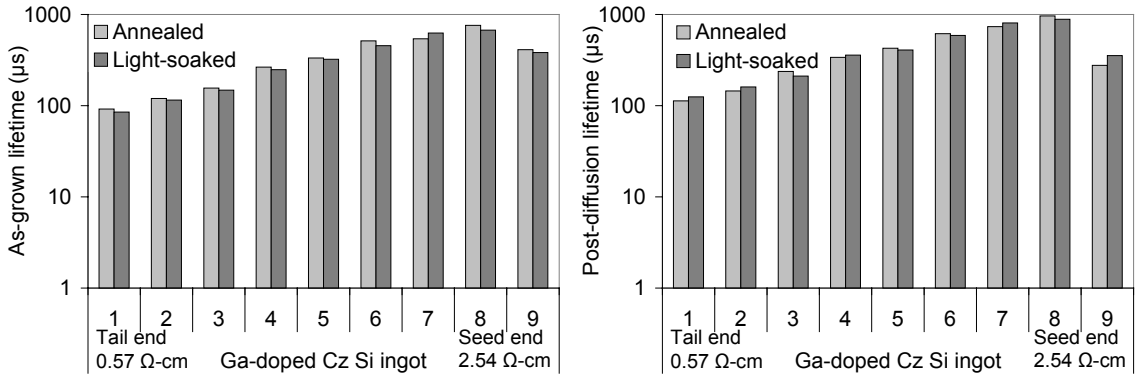


Figure 5.3 (a) As-grown and (b) post-diffusion lifetimes before and after light-soaking on wafers from different locations of the Ga-doped Cz ingot.

5.3 LID and Performance of Screen-Printed Al-BSF Solar Cells

Screen-printed Al-BSF solar cells (4 cm^2) were fabricated on all the wafers in Table 5-1 using an industrial process. First, the samples were textured in an alkaline etch and then $POCl_3$ diffused to obtain a ~45 ohm/sq emitter. Subsequently, a PECVD SiN_x layer was deposited on the front. All the samples were then subjected to full-area Al screen-printing on the backside, followed by Ag gridline printing on the front. The samples were then fired using rapid thermal processing (RTP) to form the contact and the Al-BSF. Finally, an FGA at ~400°C was performed to ensure a high-quality ohmic contact. Note that no extra heat treatment was performed to minimize the LID.

The light I-V measurements were taken after annealing the cells at 200°C to determine cell performance without the LID. The light I-V measurements were repeated on all the cells after light soaking for >20 hours to obtain stabilized cell performance after the LID.

Efficiencies of solar cells fabricated on the wafers taken from different locations of the B-doped ingot are plotted in Figure 5.4a. The efficiencies, prior to the LID, in the B-

doped ingot were quite uniform (~16.7%) except at the seed end, where the efficiency dropped slightly to 16.5%. This is entirely consistent with the lifetime data in Figure 5.1b, which shows fairly uniform lifetimes except at the seed end. However, the efficiencies of all the B-doped Cz Si cells decreased significantly by about 1.1% absolute after light soaking, resulting in a final efficiency of only ~15.6%. This is also consistent with Figure 5.1b, which shows that after the diffusion and light soaking, the lifetime in all the wafers dropped to ~20 μs after the LID.

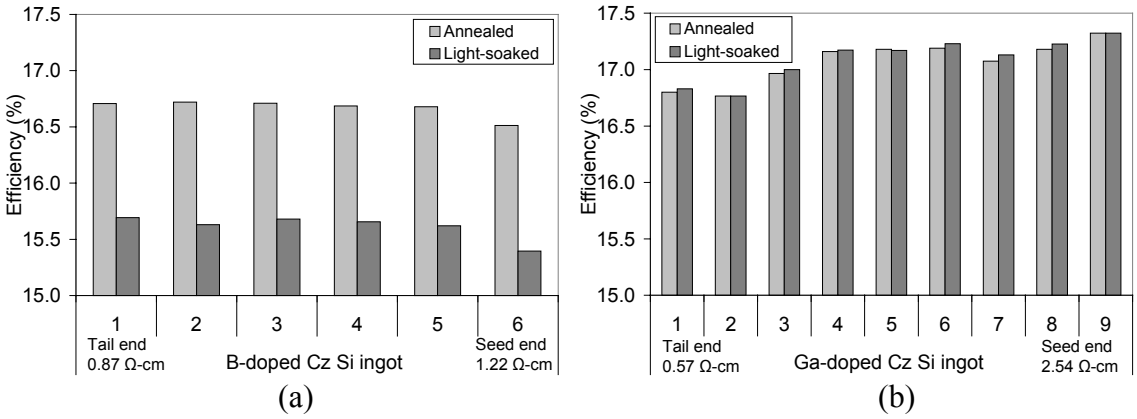


Figure 5.4 Screen-printed Al-BSF solar cell efficiency before and after light-soaking of samples from (a) the B-doped Cz Si ingot and (b) the Ga-doped Cz Si ingot.

The efficiencies of solar cells fabricated on the wafers taken from different locations of the Ga-doped ingot are shown in Figure 5.4b. Both annealed and light-soaked states are included in the figure. Compared to the B-doped ingot, the efficiency spread in the Ga-doped ingot, prior to the LID, was somewhat larger (16.8%-17.3%), with the higher-resistivity seed end producing a slightly higher efficiency. This variation in the efficiencies is generally acceptable for the production and is within the range of process-induced effects. Detailed analysis of cell parameters in Figure 5.5 shows that, in spite of

the very wide variation in resistivity over the entire length of the ingot, the spread in Ga-doped cell efficiencies is reduced because of the increase in the V_{oc} and the corresponding decrease in the short circuit current density (J_{sc}) as the resistivity decreases. Additionally, there was essentially no detectable LID observed in the Ga-doped cells, resulting in about 1.5% higher absolute efficiency after light soaking in the Ga-doped Cz Si ingot relative to the B-doped Cz Si ingot. These results confirm that Ga-doped Cz Si offers great potential for higher stabilized Cz Si cell performance. In addition, a high-quality Ga-doped ingot can be grown in the same puller used for a B-doped ingot, without any modification.

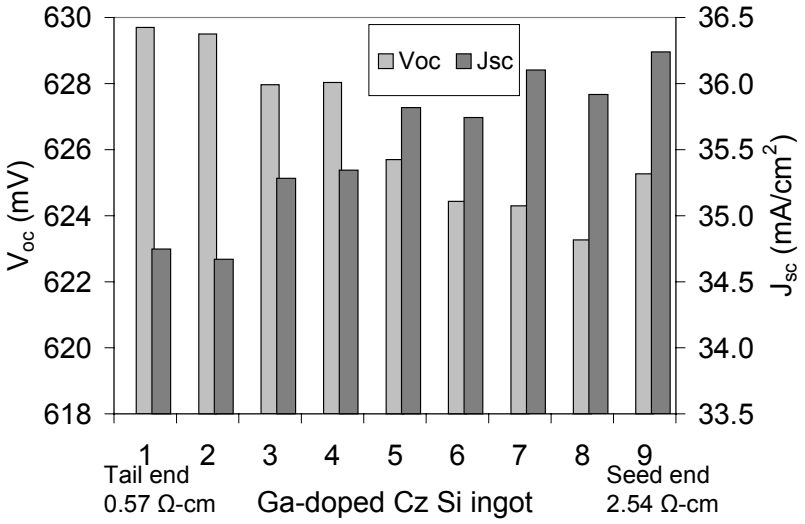


Figure 5.5 V_{oc} and J_{sc} of solar cells as a function of the ingot position in the Ga-doped ingot.

5.4 Conclusions

Substituting a Ga dopant for B in p-type Cz Si offers a great opportunity to achieve high-efficiency Si solar cells with no LID. Despite the large resistivity and lifetime variations (0.57-2.54 ohm-cm and 100-1000 μs) in the Ga-doped Cz Si ingot in this

study, the absolute efficiency of screen-printed Al-BSF solar cells was found to vary by less than 0.5% absolute (ranging from 16.8-17.3%) over the entire length of the 925 mm long ingot. Additionally, the Ga-doped Cz Si cells showed no LID at all. On the other hand, much tighter resistivity and lifetime control was observed for the 1 ohm-cm B-doped Cz Si ingot (0.87-1.22 ohm-cm and 300-400 μs). However, the lifetimes decreased from 300-400 μs to ~20 μs after the LID, resulting in degradation in the cell efficiencies of 1.1% absolute (from 16.7% to 15.6%). As a result, the 0.5-2.5 ohm-cm Ga-doped Cz Si cells gave about 1.5% higher average stabilized efficiency compared to the cells made on the 1 ohm-cm B-doped Cz Si cells.

CHAPTER 6

INVESTIGATION OF THE POTENTIAL AND THE LIMITATIONS OF THE FULL-AREA SCREEN-PRINTED AL-BACK SURFACE FILED FOR BACK SURFACE PASSIVATION

The screen-printed Al-BSF has been the preferred method in the PV industry for back surface passivation of p-type Si solar cells. Theoretical calculations show that Al-BSF has the potential to provide high-quality back surface passivation (down to a back surface recombination velocity (BSRV) of 100 cm/s) [23]. However, this has not been proven in practice. In this chapter, several practical aspects of the screen-printed Al-BSF are investigated to explore the potential and the limitations of such a technique. These include the effects of surface texturing, O content in Si, and the combined effect of the deposited Al thickness and the peak alloying temperature.

6.1 Effect of Surface Texturing

Surface texturing is widely used to minimize the front surface reflection and to enhance optical confinement in solar cells. The most common technique for surface texturing of monocrystalline Si is alkaline etching, which forms pyramids on (100) oriented crystalline Si. This technique is typically implemented in the PV industry without protecting the back surface and, therefore, results in textured surface on both sides of the cell. The impact of the textured surface on the quality of the screen-printed Al-BSF has never been quantified. To investigate the quality of the screen-printed Al-BSF on a textured surface, complete solar cells were fabricated with textured and planar

back surfaces. First, alkaline texturing was performed on both sides of 4-5 ohm-cm B-doped Cz Si samples. The samples were then diffused to obtain a 45 ohm/square emitter, followed by a SiN_x deposition on the front side. To prepare samples with a planar back surface, 30% KOH solution heated to 90°C was used to etch away the textured structure on the backside, while the front surface was protected by a SiN_x layer. To ensure that KOH etching did not affect the SiN_x antireflection property, front surface reflectance was measured before and after etching, which showed a negligible change.

It was shown in [108, 109] that a faster alloying ramp-up rate helps in obtaining uniform wetting, resulting in a more uniform Al-BSF. Therefore, in this study, the effect of the ramp-up rate was also investigated. First, ~25 μm thick Al was printed on samples with planar or textured back surfaces. They were then annealed in an RTP system with ramp-up rates in the range of 10°C/s to 100°C/s. The peak temperature and the dwelling time were fixed at 850°C and two minutes, respectively. Subsequently, front contacts were formed by Ag gridline screen-printing on the front and firing in a belt furnace, followed by an FGA.

The quality of the BSF was assessed by V_{oc} and long-wavelength internal quantum efficiency (IQE) measurements. Additionally, cross-section scanning electron microscope (SEM) pictures of the Al-BSF were taken to study the Al-BSF thickness and its uniformity. Prior to the SEM measurements, samples were broken along the crystal direction followed by etching in 1:3:6-HF:HNO_3:CH_3COOH for 10 s. The purpose of this etching is to delineate the Al-BSF (heavily p-doped) from the bulk (lightly p-doped) region [110]. All the SEM pictures were taken perpendicularly to the cross-section area of the cut wafers.

6.1.1 Impact of the Al Alloying Ramp-Up Rate on V_{oc} and IQE of Solar Cells with Textured and Planar Back Surfaces

V_{oc} of solar cells with different Al alloying ramp-up rates are shown in Figure 6.1. The data clearly show that a higher ramp-up rate produces higher V_{oc} for textured back samples. The ramp-up rate of 100°C/s gave as much as 15 mV higher V_{oc} compared to that using a 20°C/s ramp-up rate. However, a much smaller variation in V_{oc} was observed (≤ 5 mV) when the ramp-up rate was varied from 20°C/s to 100°C/s for the planar back cells.

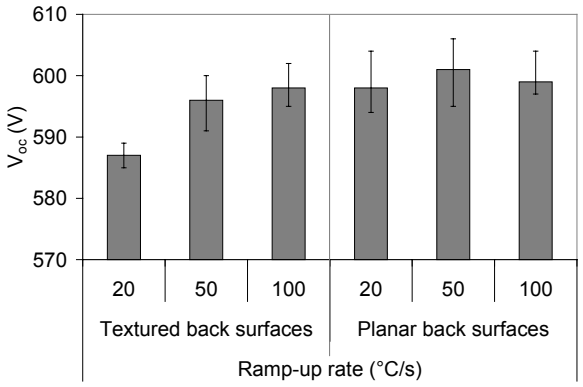


Figure 6.1 V_{oc} of Al-BSF solar cells with textured and planar back surfaces for different Al-BSF alloying ramp-up rates. The Al-printed thickness was fixed at 25 µm.

Figure 6.2a and Figure 6.2b show the long-wavelength IQE responses of the cells with textured and planar back surfaces, respectively. The IQE data are in good agreement with the measured V_{oc}. For the textured back cells, the IQE response improved significantly with faster ramp-up rates. On the other hand, an increase in the ramp-up rate did not have as much impact on the IQE response of the planar back cells. Nevertheless, a small improvement in the IQE response was observed initially when the ramp-up rate was increased from 20°C/s to 50°C/s for the planar back cells. The corresponding difference was quite significant for the textured back cells. Thus, for a printed thickness

of ~25 μm, the IQE data showed that a ramp-up rate of 50°C/s is fast enough to alloy the Al uniformly on planar surfaces but a ramp-up rate as high as 100°C/s may be required to get the best result on textured surfaces.

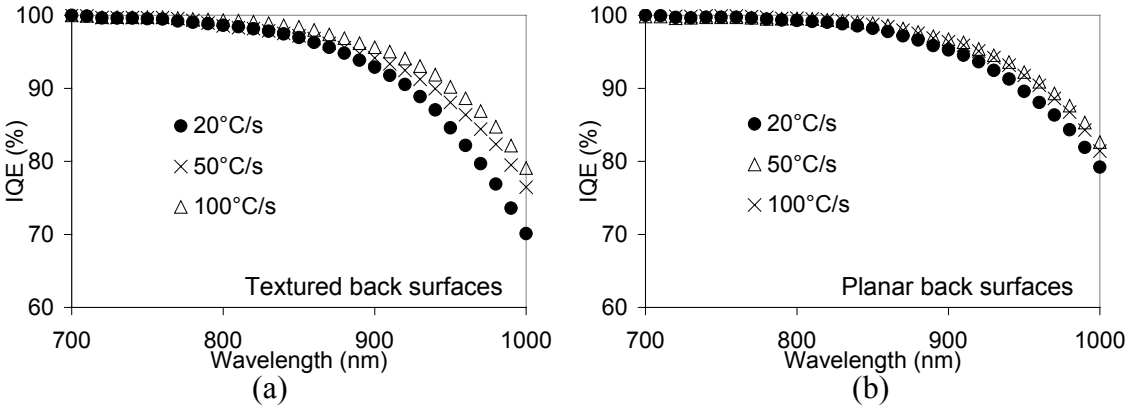


Figure 6.2 Long-wavelength IQE responses of Al-BSF solar cells alloyed at different ramping up rates with (a) textured back surfaces and (b) planar back surfaces.

6.1.2 SEM Micrographs of the Al-BSF on Textured and Planar Back Surfaces with Different Al Alloying Ramp-Up Rates

In addition to the V_{oc} and the IQE measurements, uniformity of the Al-BSF was also examined by a detailed SEM analysis of Al-BSF samples that were fabricated with ramp-up rates of 10°C/s, 20°C/s, 50°C/s, and 100°C/s (see Figure 6.3). Uniformity was judged on the basis of the BSF thickness and disconnections in the BSF layer. It is clear from Figure 6.3 that the uniformity of Al-BSF improves with the increase in the ramp-up rate for both planar and textured surfaces. For the same ramp-up rate, planar samples consistently gave a BSF with superior uniformity than textured samples, except at 100°C/s where both of them showed no disconnection in the BSF region. Interestingly, while 50°C/s gave a BSF layer without any discontinuity on the planar sample, there were still disconnections observed on the textured sample. From these results, it appears

that there is a threshold value for the ramp-up rate, below which the Al-BSF region tends to become discontinuous. In addition, this threshold value is higher for textured back surfaces. This study shows that, for Al printed thickness of ~25 μm, the threshold values of the ramp-up rate for achieving a uniform Al-BSF on textured and planar back surfaces are 100°C/s and 50°C/s, respectively.

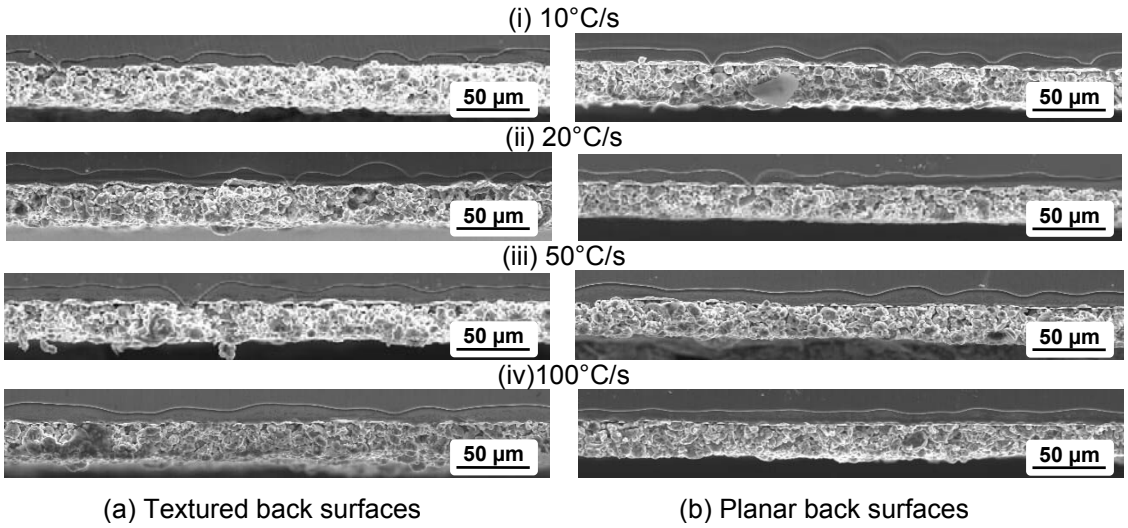


Figure 6.3 Cross-section SEM pictures of the Al-BSF formed in an RTP system with varying ramp-up rates on (a) textured surfaces and (b) planar back surfaces

6.2 Effect of Oxygen Content in Si

Single crystalline Si grown by the Cz method typically contains high amount of O_i because of the use of silica as a crucible. The high O_i content can be beneficial or detrimental based on device applications and processing conditions. Precipitation of excess O_i outside the active region can be used to form a gettering site to extract impurities from the active region [111]. On the other hand, precipitation in the active region can be detrimental to device performance [112-114]. To investigate the effect of O_i content in Si on the quality of the screen-printed Al-BSF, screen-printed Al-BSF cells

were fabricated and analyzed on four different single crystalline Si materials with varying O_i concentrations. Descriptions of the materials along with their as-grown O_i concentrations and resistivity values are summarized in Table 6-1.

Table 6-1 Summary of single crystalline Si materials with different O_i concentrations used in the study.

	FZ			MCz	B-doped Cz		Ga-doped Cz	
Resistivity (ohm –cm)	0.7	1.4	2.5	1.2	0.8	1.1	1.2	2.1
As-grown O_i (ppma) (Measured at)	-	-	-	1.26 (GT*)	13.6 (GT)	16 (NREL**)	18 (NREL)	19 (NREL)

* GT: Georgia Institute of Technology
** NREL: National Renewable Energy Laboratory

Complete solar cells were fabricated on these samples and analyzed to understand the role of O_i, if any, on the quality of the Al-BSF, V_{oc} and cell efficiency. First, all the samples were $POCl_3$ diffused to obtain a 45 ohm/sq emitter. Subsequently, a SiN_x layer was deposited on the front surface. All the samples were then subjected to full-area Al screen-printing on the backside followed by Ag gridline printing on the front. The samples were then fired in an RTP system to form the contact and the Al-BSF, followed by an FGA to ensure good ohmic contact. The solar cells were analyzed in terms of V_{oc} and long-wavelength IQE. Both the V_{oc} and the IQE measurements were performed after a 200°C anneal for the B-doped Cz Si cells to eliminate any LID effect on the bulk lifetime, so the analysis can focus only on the effect of O_i content. Finally, the BSRV was extracted by matching measured and simulated IQE using the widely used device simulation program called PC1D [115]. Note that the measured bulk lifetime was used as one of the inputs in the PC1D program.

6.2.1 V_{oc} of Solar Cells Fabricated on Different Single Crystalline Si Materials with Different O_i Concentrations

V_{oc} is plotted in Figure 6.4 as a function of resistivity for various single crystalline Si materials used in this study. It is clear that the single crystalline cells with high O_i concentrations (i.e., B- and Ga-doped Cz Si) exhibited significantly lower V_{oc} compared to the ones with low O_i concentrations (i.e., FZ and MCz Si). These data suggested that the presence of O_i in Si enhances the recombination in the screen-printed Al-BSF cells. This could be the result of bulk or surface recombination, which is decoupled in the following sections.

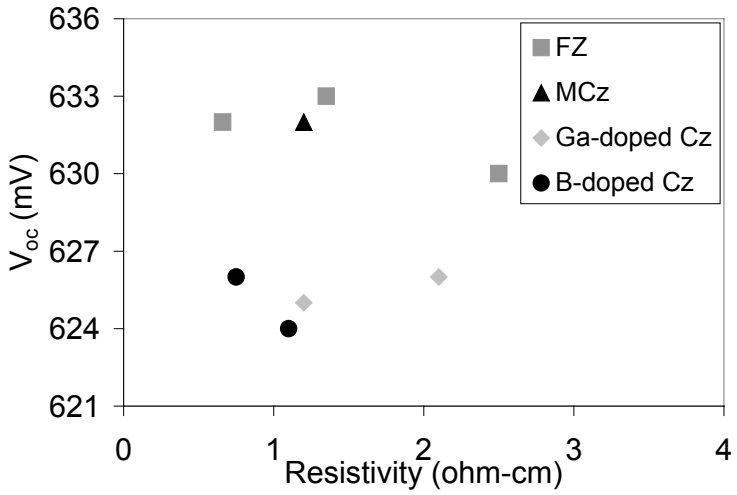


Figure 6.4 V_{oc} of solar cells as a function of resistivity for different single crystalline Si materials with different O_i concentrations.

6.2.2 IQE Analysis

IQE was measured on the cells with resistivity in the range of 1.1-1.4 ohm-cm. Figure 6.5 shows that the B- and Ga-doped Cz Si cells exhibited inferior long-wavelength IQE compared to the FZ and MCZ cells, while the short wavelength IQE was identical for all four cells (not shown in the figure). This indicated that O_i influences either the bulk lifetime or the BSRV (both of which influence the long-wavelength IQE response). An

analysis to separate the BSRV and the bulk lifetime values in these cells is discussed in the next section.

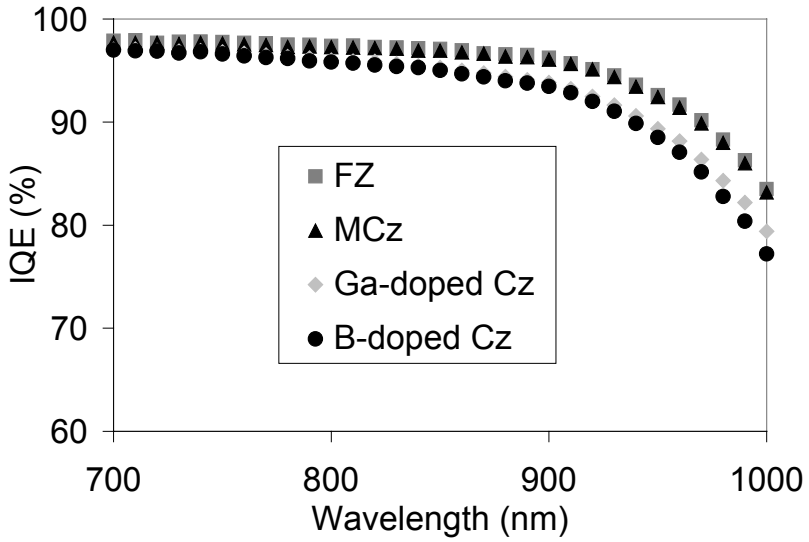


Figure 6.5 IQE of solar cells made on different single crystalline Si materials with different O_i concentrations. The resistivity of these samples is in the range of 1.1-1.4 ohm-cm.

6.2.3 Extraction of Bulk Lifetime and BSRV

The bulk lifetime in the finished cells was measured by the contactless photoconductance decay measurement after etching the cells down to bare Si. Subsequently, the BSRV was extracted by matching the measured long-wavelength IQE with the simulated IQE, using the PC1D program with the measured bulk lifetime as one of the inputs. The measured bulk lifetime and the extracted BSRV values are summarized in Table 6-2. Additionally, the BSRV values are plotted as a function of resistivity in Figure 6.6.

Table 6-2 Lifetimes and BSRV values for different single crystalline Si materials with different O_i concentrations.

Resistivity (ohm-cm)	Material	As-grown O_i (ppma)	Lifetime (μs)	BSRV (cm/s)
0.65-0.80	FZ	-	245	600
	B-doped Cz	13.6	275	1,100
1.1-1.4	FZ	-	1,400	350
	MCz	1.26	2,100	325
	B-doped Cz	16	410	675
	Ga-doped Cz	18	630	600
2.0-2.5	FZ	-	3,070	200
	Ga-doped Cz	19	1,470	400

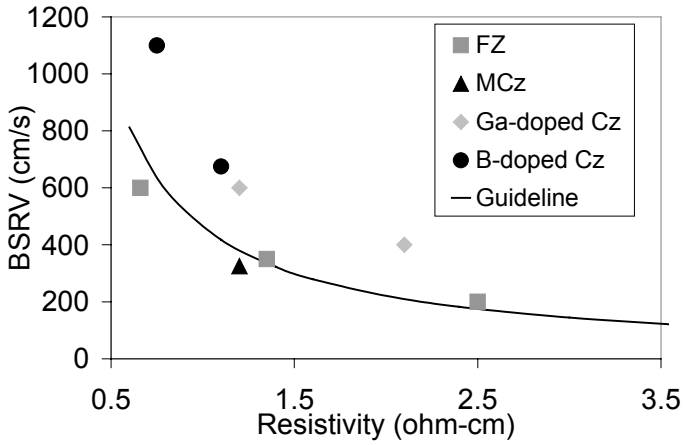


Figure 6.6 BSRV as a function of resistivity for different single crystalline Si materials with different O_i concentrations.

Table 6-2 and Figure 6.6 show that the cells fabricated on single crystalline Si with high O_i contents exhibited higher BSRV values than the low-O_i Si materials. In addition, the lifetimes in all the cells are reasonably high indicating that the long-wavelength IQE is, in fact, dominated by the back surface recombination. Thus, it appears that the BSRV increases because of the presence of high O in Si.

Higher BSRV values because of the high O_i content cannot be explained by the simplified lo-hi junction theory, which predicts that the BSRV is dictated by the doping profile and base doping. Since the recombination within the BSF region is mainly dominated by the Auger recombination, the presence of any O precipitation should not affect the lifetime in the BSF region appreciably. The higher back surface recombination is most likely a result of the O enhanced recombination within the high electric field region at the p-p^+ interface. The enhanced recombination by O-precipitation defects has been reported by several investigators for the p-n junction [112-114], which also has a high electric field.

6.3 Effect of the Al Printed Thickness and the Peak Al-Si Alloying Temperature on the Passivation Quality of the Screen-Printed Al-BSF

It is known that a thicker Al-BSF with a higher p^+ doping level generally provides a higher quality BSF. Theoretically, a thicker screen-printed Al-BSF can be obtained by either increasing the thickness of the printed Al or increasing the peak alloying temperature, while the doping level can be increased by increasing the peak alloying temperature [21, 23].

Following the models to calculate the Al-doping profile for a given temperature and deposited Al thickness given in [19] and the effective BSRV calculation given in [116, 117], the BSRV for different combinations of Al thicknesses and peak alloying temperatures was calculated. This is shown in Figure 6.7. The calculations suggest that the BSRV can be reduced either by increasing the deposited Al thickness and/or the peak alloying temperature. However, it will be shown in this section that, in practice, there exists a critical temperature for a given screen-printed Al thickness, above which the Al-

BSF layer becomes highly non-uniform. Such a phenomenon is investigated in detail both in terms of the onset conditions and its effect on solar cell performance.

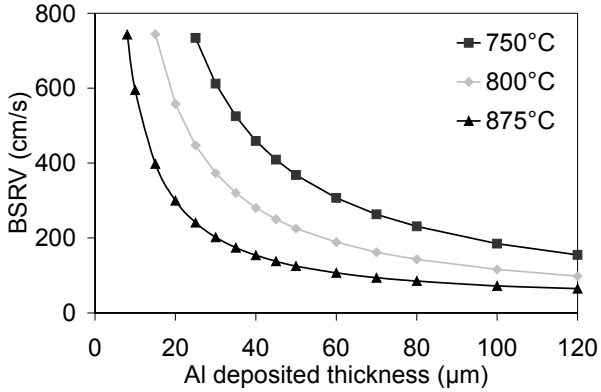


Figure 6.7 Calculated BSRV as a function of deposited Al thicknesses for different peak alloying temperatures on a 1.3 ohm-cm p-type substrate.

6.3.1 Formation and Observation of the Non-Uniform Al-BSF above a Critical Alloying Temperature

This section shows that when the peak Al-Si alloying temperature exceeds a critical value, large numbers of bumps are formed on the external Al surface (Figure 6.8). In addition, the size of these bumps becomes larger with increased Al thicknesses. To ensure that this phenomenon is not specific to the particular Al paste being studied, three additional Al pastes were printed and fired above the critical temperature. The distributed Al bumps were observed for all the four pastes (Figure 6.9), indicating that the agglomeration is not a paste-dependent phenomenon.

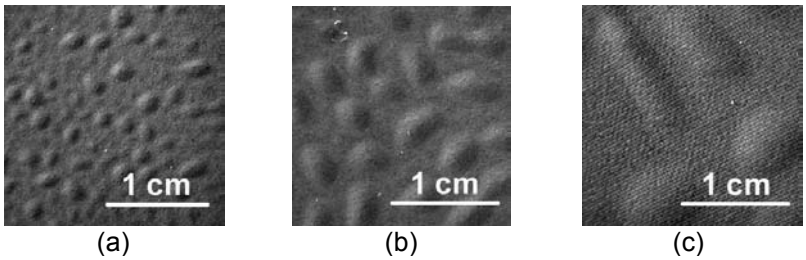


Figure 6.8 Formation of bumps on post-fired Al surfaces after a 925°C heat treatment for Al thicknesses of (a) 24μm, (b) 40 μm, and (c) 62 μm.

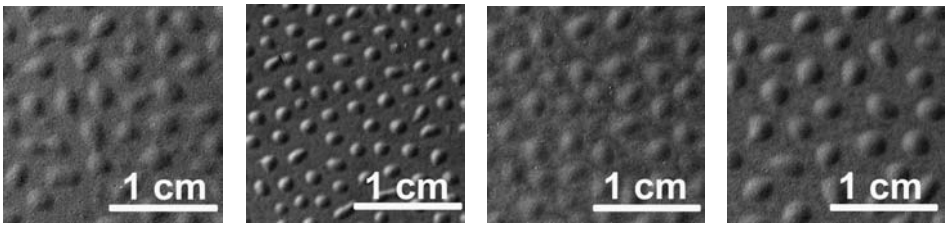


Figure 6.9 Formation of bumps on post-fired Al surfaces for four different Al pastes after a 925°C heat treatment. Al thicknesses are in the range of 30-40μm.

To examine the impact of these bumps on the uniformity and the quality of the Al-BSF, cross-sectional SEM micrographs were taken at and around a bump on the sample with 24-μm thick Al fired at 925°C for 5 s in an RTP system (with a ramp-up rate and a ramp-down rate of 50°C/s and 30°C/s, respectively) (Figure 6.10). The SEM cross-section in Figure 6.10 clearly shows that the Al-BSF is very thick underneath the peak of the bump (~20 μm); however, the Al-BSF around the bump, or slightly away from it, is very thin (~4 μm). The region between the bumps but further away from them has a moderately thick BSF (~13 μm), which represents the average thickness of the Al-BSF. This cross-sectional morphology and the Al-BSF melt and re-growth process suggests that this non-uniform BSF occurs as a result of the agglomeration of the Al-Si melt at a certain temperature for a given deposited Al thickness. A large amount of melt at the agglomerated region leads to a depleted molten region around the bumps. When the sample cools down, the re-growth of the Al-BSF region is very non-uniform, with a thick BSF region near the peak of the bumps, surrounded by very thin BSF regions. A schematic of the proposed model to explain the observed non-uniform BSF formation above a critical temperature is shown in Figure 6.11.

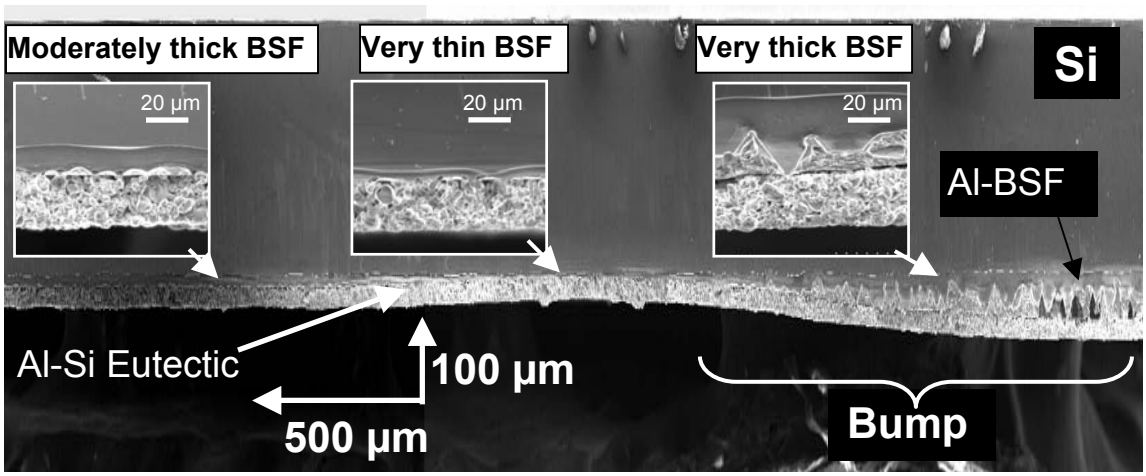


Figure 6.10 Cross-sectional SEM micrograph of a bump (agglomerated) region of a Si sample with 24-µm thick Al annealed at 925°C in an RTP system.

The Al-bump formation is likely related to the wetting phenomenon. The driving force for the agglomeration may be related to the reduction of the interface energy between the Al/Si melt and Si by minimizing the contact interface area. This happens via the formation of a higher contact angle, which produces the bumps.

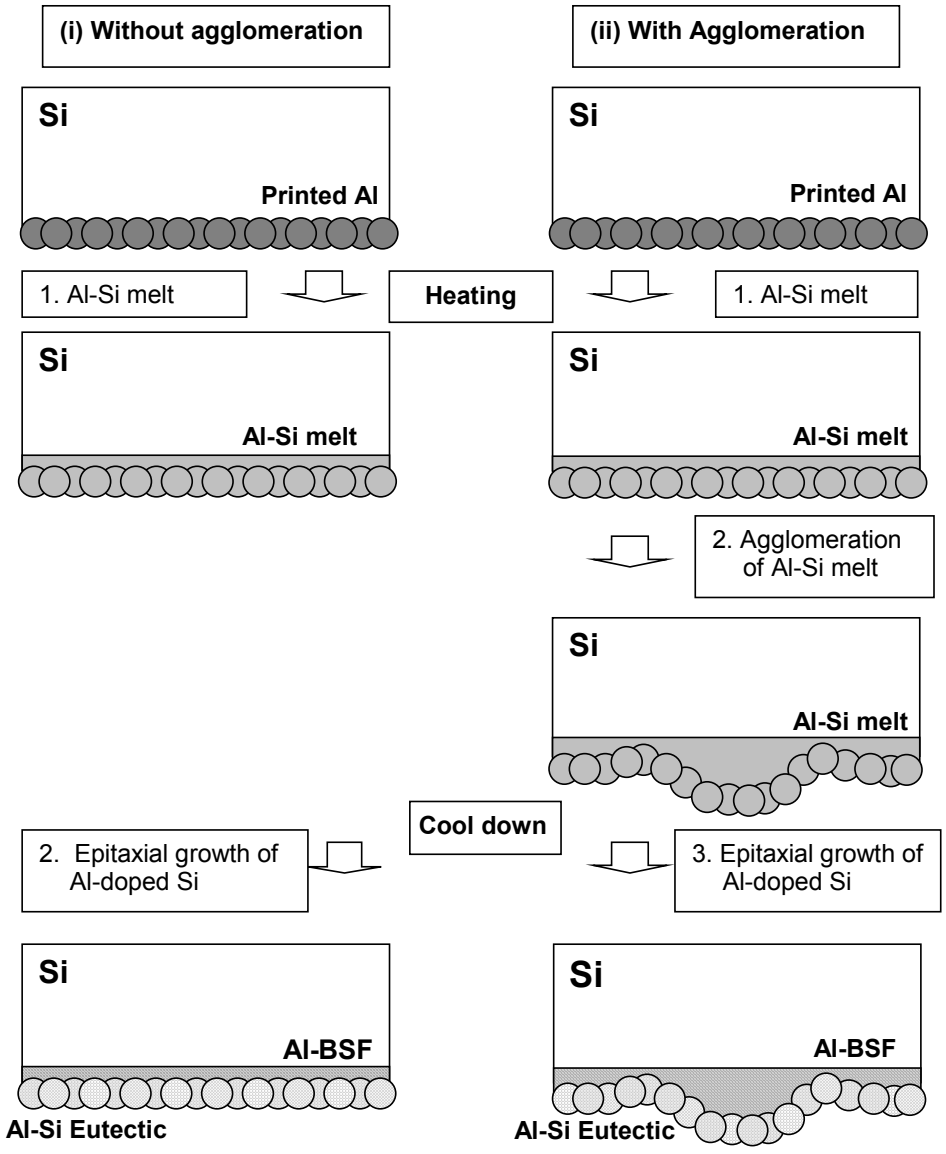


Figure 6.11 Schematic of the proposed model for the observed Al agglomeration. The regular melt and re-growth process without the agglomeration is included for comparison.

6.3.2 Determination of the Critical Temperature for the Onset of Agglomeration for a Given Al Thickness

Attempts were made to identify a critical temperature at which the agglomeration begins to occur. Three different screen meshes were used to obtain three different Al printed thicknesses of 24 μm, 40 μm, and 62 μm (thicknesses were measured by SEM after printing, drying, and firing). The alloying was performed in an RTP system to

provide an accurate measure of the firing profile. A ramp-up rate of 50-75°C/s was used along with the dwelling time of 5-20 s at the peak temperature. The ramp-down rate was set to ~30°C/s. The peak temperature was varied from 700 to 925°C in 25°C increments. For quantitative comparison, the onset of agglomeration was defined when the thickness of the Al-BSF under the bump became 20% greater than the average Al-BSF thickness. The critical temperatures for 24, 40, and 62 μm thick Al were determined by SEM analyses. Figure 6.12 shows a curve that gives the highest temperature at which a given thickness of Al can be fired without the agglomeration. This limits one's ability to take a full advantage of a higher alloying temperature to increase the Al-BSF thickness and doping, which reduces the BSRV. Likewise, once the firing temperature is selected, one cannot increase the Al thickness beyond a certain level because of the agglomeration phenomenon. The following section shows the quantitative impact of the agglomeration on the V_{oc} of screen-printed Al-BSF solar cells.

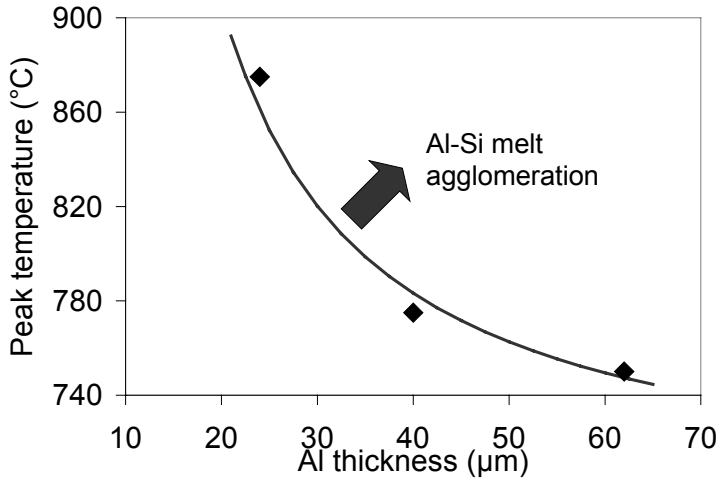


Figure 6.12 Highest allowed peak alloying temperatures and corresponding Al printed thicknesses (measured after firing) to avoid the agglomeration of the Al-Si melt.

6.3.3 Effect of the Agglomeration of the Al-Si Melt on the BSF Quality and Solar Cell Performance

To examine the effect of the non-uniform BSF caused by the agglomeration, screen-printed Al-BSF solar cells were fabricated on 300-μm thick 1.3 ohm-cm p-type FZ Si with several combinations of temperatures and Al printed thicknesses. First, a 45 ohm/sq n^+ emitter was formed by 880°C $POCl_3$ diffusion. Following P-glass removal, a PECVD SiN_x layer was deposited on the front surface. Samples were then subjected to full-area backside Al screen-printing using a commercially available Al paste. Subsequently, the samples were fired in an RTP system at different peak temperatures (with the same dwelling time, ramp-up and ramp-down rates as discussed in the previous section) to have ten different combinations of Al thicknesses and peak alloying temperatures (shown in Figure 6.13). Finally, the Ag gridlines were screen printed on the front, followed by front contact firing in an RTP system at ~718°C (with a ramp-up rate of ~75°C, a dwell time of 2 s and a ramp-down rate of ~30°C) and an FGA at 400°C for about 20 minutes. Cells were characterized by light I-V measurements, light beam induced current (LBIC) mapping [118], and IQE measurements.

6.3.4 V_{oc} as a function of Peak Alloying Temperatures and Printed Al Thicknesses

The V_{oc} of solar cells with different combinations of Al thicknesses and peak alloying temperatures is plotted in Figure 6.13, which shows that there exists an optimum peak temperature for each printed Al thickness. It is important to note that the optimum peak temperature was lower for thicker Al. The critical temperature for the agglomeration for each Al thickness (obtained from Figure 6.12) is also included in Figure 6.13 and is presented by dashed-dotted vertical lines. Note that the optimum peak temperatures for the highest V_{oc} in Figure 6.13 match very well with the critical temperatures for the

agglomeration. The trend in V_{oc} in Figure 6.13 confirmed the detrimental effect of the agglomeration of the Al-Si melt because the V_{oc} was found to decrease when the firing temperature exceeded the critical temperature. An optimal temperature exists because, below this temperature, the BSF is thin and inferior, and above this temperature, the Al melt agglomeration starts to degrade the BSF quality. It is interesting to note from Figure 6.13 that the highest V_{oc} in this study was obtained using the thickest Al (52 µm) in combination with a lower firing temperature of 750°C.

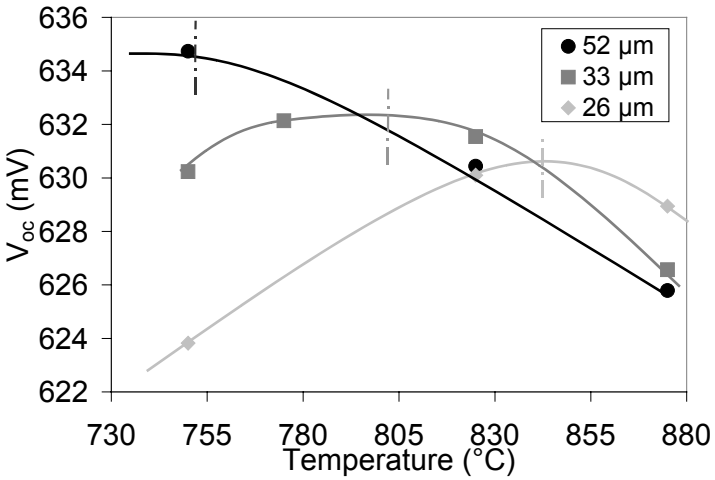


Figure 6.13 V_{oc} of solar cells as a function of peak alloying temperatures for three different Al printed thicknesses. The sold lines represent the experimental data and the dashed-dotted lines represent the onset of agglomeration for each Al printed thickness.

6.3.5 LBIC and IQE Analyses to Characterize and Understand the Impact of the Al-Si Melt Agglomeration on the BSF Quality

To gain a better understanding of the effect of the Al-Si melt agglomeration on the BSF quality, LBIC maps using a long-wavelength (980 nm) laser were obtained on four cells with different combinations of printed Al thicknesses and peak firing temperatures. The 980 nm is absorbed deep in the bulk and is, therefore, indicative of the BSRV and the bulk lifetime. Since the lifetime in the FZ Si used in this study was very high (≥ 500

μs) and uniform, variation in the LBIC response primarily reflected the variation in the BSRV. The four cells used for the LBIC analysis were fabricated with (a) 26-μm thick Al fired at 750°C, (b) 26-μm thick Al fired at 875°C, (c) 52-μm thick Al fired at 750°C, and (d) 52-μm thick Al fired at 875°C.

The LBIC maps of these cells are shown in Figure 6.14. The LBIC response is in very good agreement with the V_{oc} data. It shows that for the 26-μm thick Al, which has a critical temperature of 850°C (Figure 6.13), an increase in the firing temperature from 750°C to 875°C resulted in a uniform increase in the LBIC response over the entire cell area. This is attributed to the increase in the Al-BSF thickness in conjunction with negligible amount of the agglomeration. However, in the case of 52-μm thick Al (critical temperature=750°C), an increase in the firing temperature from 750°C to 875°C reduced the LBIC response significantly. In addition, a non-uniform LBIC response was observed for this sample because of the melt agglomeration. Interestingly, the region away from the bumps, which was found to have moderately thick BSF, showed a lower response than the 750°C fired sample. Finally, contrary to the expectation, the agglomerated regions with a very thick BSF showed an even lower LBIC response compared to the thinner BSF region away from the bumps.

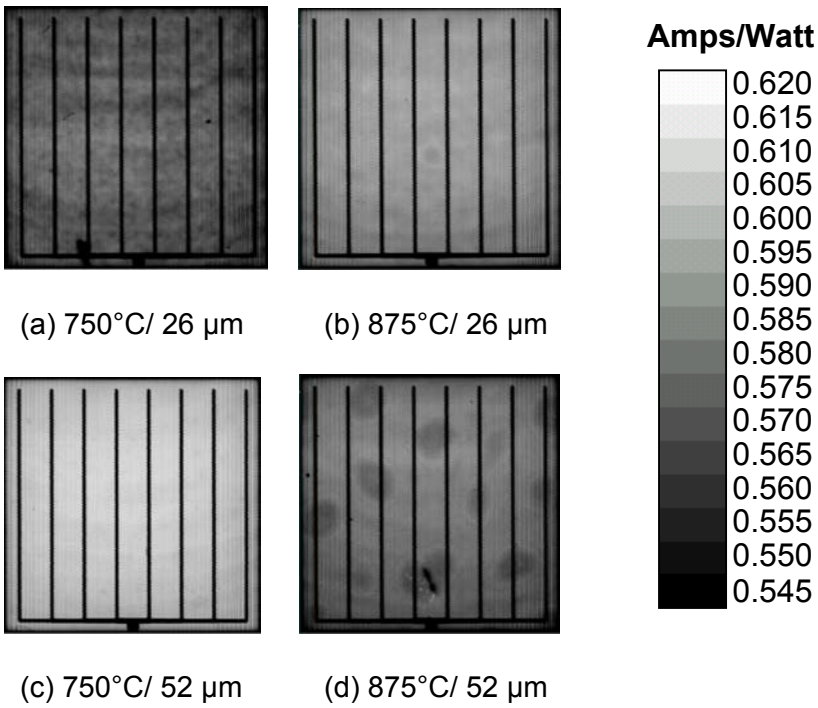


Figure 6.14 LBIC responses at 980 nm of four cells with different Al-BSF formations: (a) T_{peak}: 750°C, Al thickness: 26 µm, (b) T_{peak}: 875°C, Al thickness: 26 µm, (c) T_{peak}: 750°C, Al thickness: 52 µm, and (d) T_{peak}: 875°C, Al thickness: 52 µm.

To further enhance the understanding of this phenomenon, IQE measurements were performed on the above four samples, IQE was done only on one spot for the three samples that did not exhibit the agglomeration. On the fourth sample with the agglomeration (T_{peak}: 875°C, Al thickness: 52 µm), the IQE measurements were taken at two locations: inside and outside the agglomerated region. All five IQE responses are plotted in Figure 6.15 in the 700-1,000 nm wavelength range, which is most sensitive to the bulk lifetime and the BSRV.

The IQE data were in very good agreement with the LBIC measurements. For the cell with 52-µm thick Al fired at 875°C, the IQE response between the agglomerated regions was found to be lower than the IQE response of the sample fired at a low temperature of 750°C (with no agglomeration). Consistent with the LBIC data, the IQE data also showed

that the agglomerated thick Al-BSF region had a lower IQE response compared to the thin Al-BSF region further away from it. Notice that the sample with 26-μm thick Al fired at 750°C gave the lowest IQE response because 750°C is well below the optimum firing temperature of 850°C for this Al thickness.

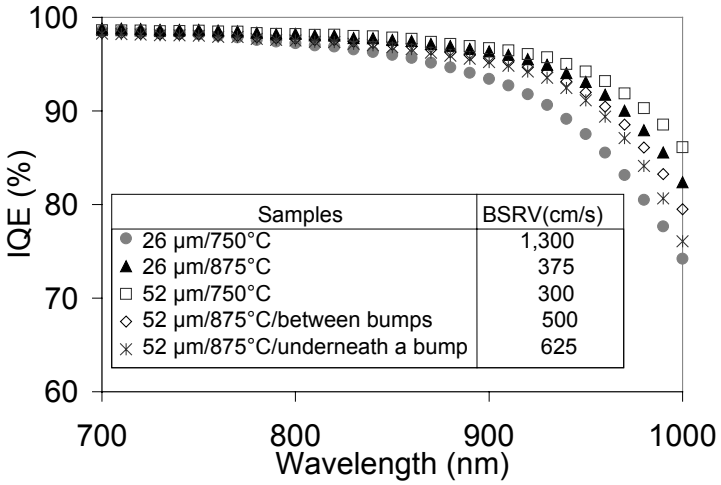


Figure 6.15 IQE responses from 700-1,000 nm of the four samples in Figure 6.14.

The measured IQE data were matched with the calculated IQE data from the PC1D program to extract the BSRV from the IQE curve. The matching was done only in the wavelength range of 800-940 nm because it is most sensitive to the bulk lifetime and the BSRV. Since the bulk lifetime of the FZ Si used in this study was very high (≥500 μs), the IQE response in the above wavelength range is primarily dictated by the BSRV. The extracted BSRV values are also shown in Figure 6.15.

6.3.6 Determination of Al-BSF Profiles by an Electrochemical C-V (ECV) Measurement to Understand the Effect of the Al-Si Melt Agglomeration on the BSF Quality

Conventional wisdom says that 52-μm thick Al fired at 875°C should give the best BSF quality. Figure 6.15 in the previous section showed that this was not the case. To

understand the reason for the lower IQE and LBIC responses of this sample, electrically active p^+ profiles of the Al-BSF were obtained by ECV measurements [119, 120] inside and outside the agglomerated region. For comparison, an ECV profile was also measured on the sample with 52-µm thick Al fired at 750°C. The three p^+-doping profiles are shown in Figure 6.16. The ECV measurements were performed with an 8-mm diameter sealing ring. The two spots used for the ECV measurements on the 52-µm thick Al fired at 875°C are depicted in Figure 6.16 as well.

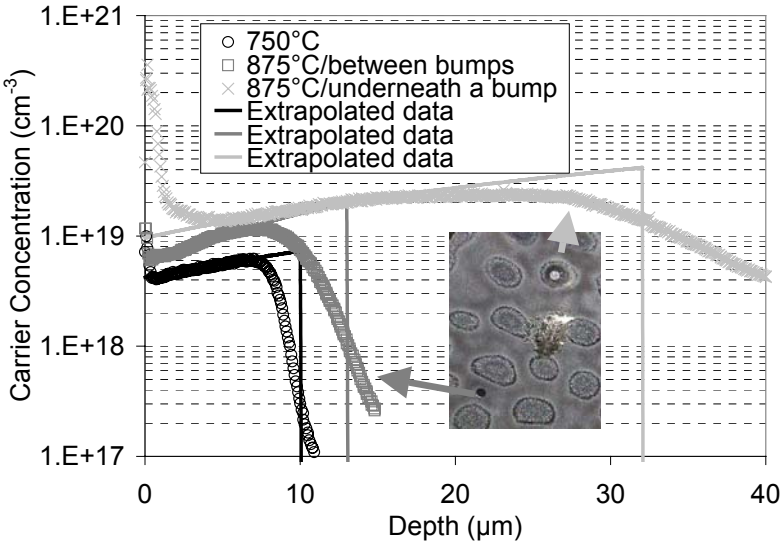


Figure 6.16 Electrically active p^+ profiles of the Al-BSF measured by the ECV technique in three locations: (a) an arbitrary region on the sample with a uniform BSF formed with 52-µm thick Al fired at 750°C, (b) the region underneath the bump on the sample with 52-µm thick Al fired at 875°C, and (c) the region further away from the bump on the sample with 52-µm thick Al fired at 875°C. The solid lines represent the extended profiles corrected for the underestimated thickness and peak concentration of the BSF because of the roughness of the crater front during the ECV measurement as well as the variation in the BSF thickness.

The junction depths of the Al-BSF layers shown in Figure 6.16 are quite consistent with the trend discussed in Figure 6.10: the region underneath the bump has a very thick BSF and the region between the bumps has a moderately thick BSF. The gradual decrease in the Al or p^+ concentration into the Si bulk after reaching the peak

concentration (more pronounced in the agglomerated region), instead of an abrupt junction predicted by the theory, is attributed to the spatial inhomogeneity of the crater etching front as a result of the surface roughness and the variation in the BSF thickness [21]. The peak concentration and the thickness of the BSF profile follow the trend given by the Al-Si alloying theory, where a higher temperature provides higher doping and a thicker BSF. However, the p^+ concentration, even for the 750°C sample, is quite high compared to the theoretical calculation based on the solid solubility data of Al in Si in [22] ($\leq 3\times10^{18}$ cm^{-3} for a peak firing temperature of <900°C). Nevertheless, some investigators have discussed and reported higher Al solid solubility and, hence, the Al-doping concentration in Si by the Al-Si alloying process [121, 122]. Others have attributed the higher p^+ concentration in the screen-printed Al-BSF to the B or borosilicate glass presented in the paste [123]. The spreading resistance measurements were also performed in this work that also supported this higher than expected p^+ concentration (not shown here).

To gain deeper insight into how the three profiles in Figure 6.16 should affect the quality of back surface passivation, the effective BSRV at the p-p^+ interface was calculated using these three measured profiles. To correct for the underestimated BSF thickness as well as the peak concentration of the BSF profiles because of the roughness of the crater front in the ECV measurement, the profile was extrapolated to extend the BSF thicknesses to match the thicknesses measured by cross-sectional SEM. Additionally, the abrupt junction was assumed (see Figure 6.16). The three corrected profiles, shown by the solid lines in Figure 6.16, were then used to calculate the BSRV values at the p-p^+. The calculated BSRV values for the three corrected profiles are

summarized in Table 6-3. For comparison, the extracted BSRV values by the IQE matching in Figure 6.15 are also included in the table.

Table 6-3 Comparison of the calculated BSRV values from the actual doping profiles and the extracted BSRV values from IQE matching in Figure 6.15.

Samples	Location	Calculated BSRV (cm/s)	Extracted BSRV (cm/s)
52 μm thick Al fired at 750°C	Arbitrary	144	300
52 μm thick Al fired at 875°C	Underneath a bump	310	625
	Region in between bumps	179	500

The BSRV values calculated from the doping profiles are about a factor of two lower than the experimentally extracted BSRV. This could partially be attributed to the non-ideal p-p^+ junction formed by the alloying process. Nevertheless, the BSRV trends for both cases are quite consistent with each other. The calculations show the highest BSRV for the BSF profile underneath a bump formed at 875°C, the lower BSRV for the BSF region further away from the bumps, and the lowest BSRV for the uniform BSF fired at 750°C. At first, it would seem that the calculations contradicted the BSF theory because a thicker BSF is normally expected to provide a lower BSRV. To gain better understanding of these results, additional calculations were performed to obtain BSRV values for a uniformly doped BSF with different combinations of BSF thicknesses and doping concentrations. These are plotted in Figure 6.17.

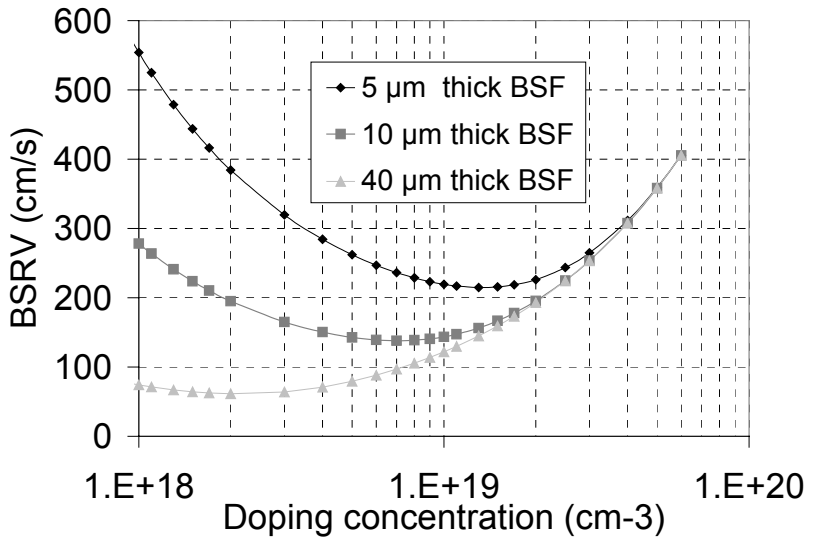


Figure 6.17 Calculated BSRV for different thicknesses of a uniformly doped BSF as a function of doping concentrations.

It can be seen from Figure 6.17 that for a reasonably thick BSF (≥10 µm) with a high doping concentration ($\geq 7\times10^{18}$ cm^{-3}), the BSRV becomes less dependent on the thickness of the BSF and increases with the doping concentration. This is because (1) a thick BSF with a high doping concentration becomes opaque to the high recombination at the metal/Si interface and (2) an increase in the doping concentration beyond 7×10^{18} cm^{-3} enhances the band gap narrowing effect (ΔV_G), which degrades the effectiveness of the lo-hi junction (refer to Chapter 2 for more detail on the effect of the band gap narrowing on the passivation quality of a lo-hi junction). Figure 6.16 shows that the peak concentrations for the three profiles exceed 7×10^{18} cm^{-3}; therefore, heavy doping in the BSF layer (or the band gap narrowing effect) dominates the BSRV trend in Table 6-3, rather than the BSF thickness. Figure 6.17 also suggests that a proper combination of the Al-BSF thickness and the peak concentration is crucial for achieving optimum Al-BSF performance. The concept of going to high temperatures to obtain higher doping cannot

be applied because the measured peak p^+ concentration exceeds 7×10^{18} cm^{-3} rather than the predicted value of less than 3×10^{18} cm^{-3} from the phase diagram [22]. Thus, a combination of the non-uniform BSF, formed as a result of the agglomeration, and the band gap narrowing effect puts a limit on high-temperature firing of thick Al layers. This produced a V_{oc} versus temperature trend shown in Figure 6.13, which favors lower temperatures with thicker printed Al.

6.4 Conclusions

In this chapter, it is shown that the ramp-up rate plays a major role in dictating the uniformity of the Al-BSF layer formed by the Al-Si alloying process. A higher ramp-up rate generally provides better uniformity. It was further observed that textured back surfaces require even a higher ramp-up rate to obtain a uniform BSF compared to planar back surfaces. For an Al printed thickness of 25 μm, a ramp-up rate of 50°C/s was sufficient to get a uniform BSF layer on planar back surfaces, but this threshold value increased to 100°C/s for textured back surfaces.

It was established that the Al-BSF cells fabricated on regular Cz Si with a high O_i content exhibited higher BSRV values compared to the low-O_i FZ Si. Further, MCz cells with a low O_i content did not show this enhanced recombination. The higher BSRV in crystalline Si materials with a high O_i content could be resulted from O precipitation induced defects within the p-p^+ junction.

It was found that there exists a critical alloying temperature for a given Al-thickness above which the Al-BSF becomes non-uniform and solar cell performance starts to degrade. This critical temperature is lower for thicker Al layers, which puts a limit on the maximum thickness of the Al-BSF that can be achieved. It was found that the non-

uniform Al-BSF is a result of the agglomeration of the Al-Si melt at higher temperatures and is responsible for a significant variation in the Al-BSF thickness. It is demonstrated that this non-uniformity in the BSF layer, in combination with the band gap narrowing effect, because of greater than expected doping, has a detrimental effect on solar cell performance. This work also showed that a proper combination of the BSF thickness and the peak doping concentration is crucial for obtaining the best passivation quality from the screen-printed Al-BSF.

The last section of this chapter revealed why, in practice, it is difficult to reach the full theoretical potential of the screen-printed Al-BSF. The higher quality BSF requires very thick Al, which tends to warp thinner substrates. In addition, the low-to-moderate reflectance (~65%) inherently associated with the Al-Si alloyed back surface is another drawback for the utilization of the Al-BSF for thinner substrates. Since thinner substrates are crucial for lower cost PV, the use of dielectric passivation with local back contacts is the best route to low-cost, high-efficiency thin cells. This is the subject of investigation in the rest of the thesis.

CHAPTER 7

DESIGN AND UNDERSTANDING OF DIELECTRIC BACK-PASSIVATED SOLAR CELLS THROUGH MULTI-DIMENSIONAL SIMULATIONS

This chapter deals with the optimum contact design and an improved theoretical understanding of dielectric back-passivated p-type Si solar cells with local back contacts through device simulations. The chapter is divided into three parts: (1) design of a local contact geometry, (2) investigation of the effect of charge in the back dielectric layer, and (3) design of a structure and a process scheme for low-cost high-efficiency dielectric back-passivated p-type Si solar cells. The first two sections involve the use of a multi-dimensional semiconductor simulation program: DESSIS^{TM}. In the first section, 2- and 3-D simulations were performed to provide guidelines for designing the back contact. The second section provides an understanding of the effect of charge present in the back dielectric layer on cell performance. Subsequently, a combination of a cell structure and a process scheme for achieving low-cost dielectric back-passivated cells is proposed in the last section.

7.1 Design of Local Back Contact Geometries for High-Efficiency Dielectric Back-Passivated Si Solar Cells

Two common geometries for back contacts were investigated: a line contact and a point contact (Figure 7.1a and b respectively). These geometries have been around but are often implemented without a comprehensive and quantitative understanding of the impact of the contact-design. This is because it requires elaborate 2 or 3-D modeling to account for all the effects. In this section, modeling was performed to develop a comprehensive understanding of such contact systems.

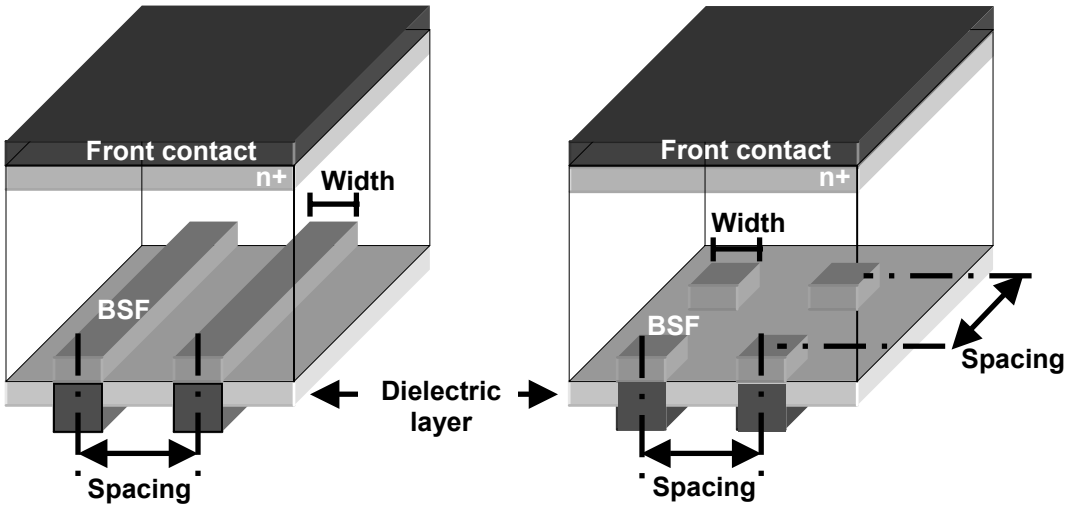


Figure 7.1 Structures used in the design of the local back contact for (a) a line contact geometry and (b) a point contact geometry.

7.1.1 Overview of the Simulation

The simulation domain was derived from the smallest unit cell that can be extended periodically to represent the complete structure. To simplify the simulation problem, an assumption of a uniformly distributed front contact was made (shown in Figure 7.1). By assuming a uniform front contact, the size of the unit cell is solely controlled by the back contact geometry. The simulation domains used for the line and the point contacts are shown in Figure 7.2a and b, respectively. The optical generation was simulated by assuming a uniform light incident on a textured Si surface with an antireflection layer that has index of 2.0 and a thickness of 75 nm. The incident one-sun light was derated by 8.5% to account for shading by a front contact in the actual devices.

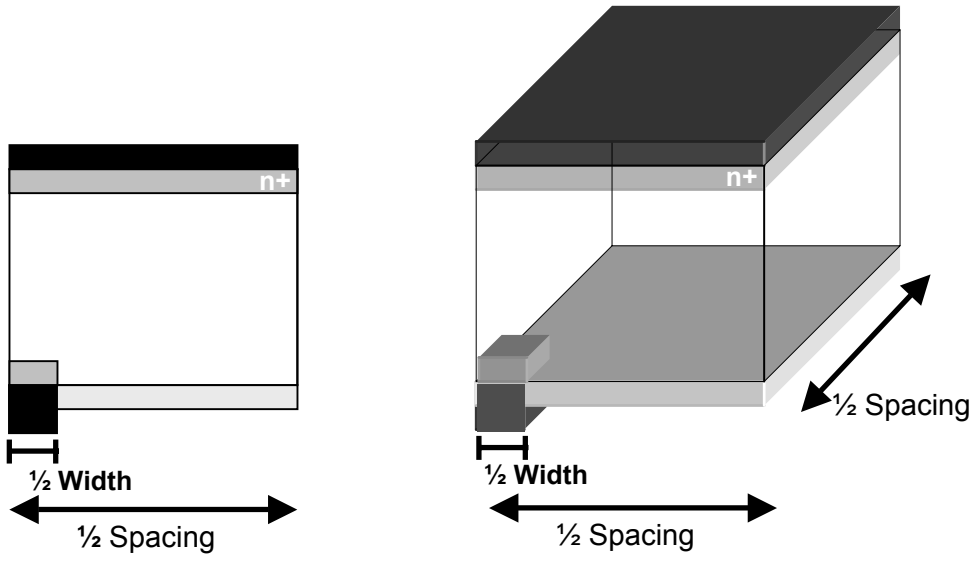


Figure 7.2 The simulation domains used for (a) a line back contact and (b) a point back contact.

Several fixed parameters used in the simulation are summarized in Table 7-1.

Table 7-1 Fixed parameters used in the design of the local back contact.

Parameters	Value
Emitter	80 ohm/sq (Gaussian profile with a surface concentration of 1.139×10^{20} cm^{-3} and a junction depth of 0.3 μm)
Cell thickness	200 μm
SRH lifetime (midgap traps: E_t=0) $\tau_{n0}=\tau_{p0}$	1,000 μs
Front SRV	60,000 cm/s
Optical generation	Textured (facet angle = 54.74°), 8.5% shading, with SiN_x (750 Å, n=2) R_{front} (internal)=0.92 R_{back} (internal)=0.85
Contact resistance	0 ohm-cm^2

Here, the variables of interest included the contact type (line or point), contact size, contact spacing, base resistivity, and the SRV at the contact. In these simulations, the SRV at the back dielectric/Si interface was varied for different base resistivity to obtain the same J_0 value of 8.17×10^{-14} A/cm^2 by using the following equation:

$$J_0 = q \cdot \frac{n_i^2}{N_A} \cdot S, \tag{7.1}$$

where n_i of 8.58×10^9 cm^{-3} was used in the calculations. The corresponding SRV values for different resistivity used in these simulations are shown in Table 7-2.

The SRV at the contact is another important parameter that affects the optimal design of the contact. Its value in practice depends on the quality of the LBSF underneath the contact as well as the base resistivity. Here, to vary the contact SRV, the LBSF layers with a constant doping concentration of 1×10^{19} cm^{-3} but with different thicknesses of 1.47, 0.35, and 0 μm were applied underneath the contact. The corresponding contact

SRV values for different base resistivity (as evaluated by the PC1D program) are summarized in Table 7-2. Note that, to avoid any complication because of the possible recombination at the edge of the back contact, the LBSF applied in these simulations was extended by 1.3 μm around the contact. The effect of this lateral LBSF is discussed in more detail in Section 7.1.5.

The variables and their values are summarized in Table 7-2. The cell efficiency was obtained by 2 & 3-D device modeling as a function of contact parameters and was used as an indicator for an optimal contact design.

Table 7-2 Variable parameters used in the design of the local back contact.

Parameters	Value
Contact type	Line or point
Contact width	75 μm or 150 μm
Contact spacing	250, 500, 1000, or 2000 μm
Resistivity	0.5, 1.0, 2.0, or 6.0 ohm-cm
SRV at the dielectric (E_t=0)	S_{n0}=S_{p0}=226 cm/s for 0.5 ohm-cm S_{n0}=S_{p0}=105 cm/s for 1.0 ohm-cm S_{n0}=S_{p0}= 50 cm/s for 2.0 ohm-cm S_{n0}=S_{p0}= 16 cm/s for 6.0 ohm-cm (The SRV was varied to obtain the same J_0 on different base resistivity) (Assume no charge in the dielectric)
Effective SRV at the contact	1350, 4500, or 10^6 cm/s for 0.5 ohm-cm 625, 2100, or 10^6 cm/s for 1.0 ohm-cm 300, 1000, or 10^6 cm/s for 2.0 ohm-cm 95, 320, or 10^6 cm/s for 6.0 ohm-cm (This was achieved by introducing LBSF layers with fixed doping of 1×10^{19} cm^{-3} and thicknesses of 1.47, 0.35, and 0 μm, respectively) Note: lateral BSF of >1.3 μm is applied unless mentioned otherwise

7.1.2 Understanding the Effect of the Contact Spacing for the Point and the Line Back Contact Geometries

Figure 7.3 shows simulated solar cell efficiency as a function of contact spacing and SRV values at the contact for contact widths of 75 and 150 μm for the point and the line back contact geometries on 2.0 ohm-cm substrates. Although only the case of 2.0 ohm-cm substrates is considered here, it is expected that the discussions given in this section apply to other resistivity values as well.

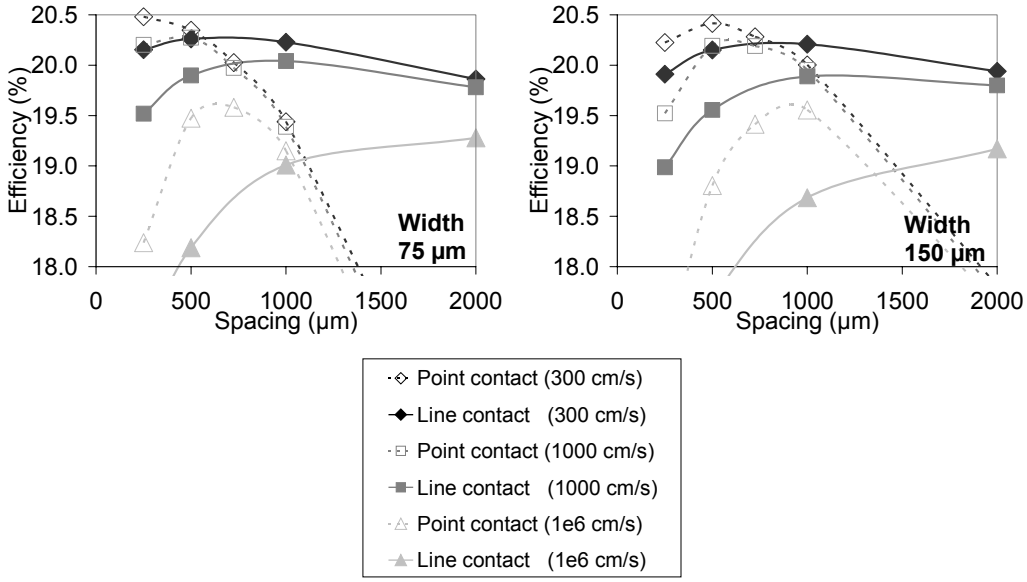


Figure 7.3 Simulated solar cell efficiency for the line and the point contact structures for contact widths of 75 and 150 μm and contact recombination velocities of 300, 1,000, 10^6 cm/s on 2.0 ohm-cm substrates.

Additionally, J_{sc}, V_{oc}, and fill factor (FF: the product of I and V at the maximum power point of a solar cell divided by the product of I_{sc} and V_{oc}) are plotted in Figure 7.4.

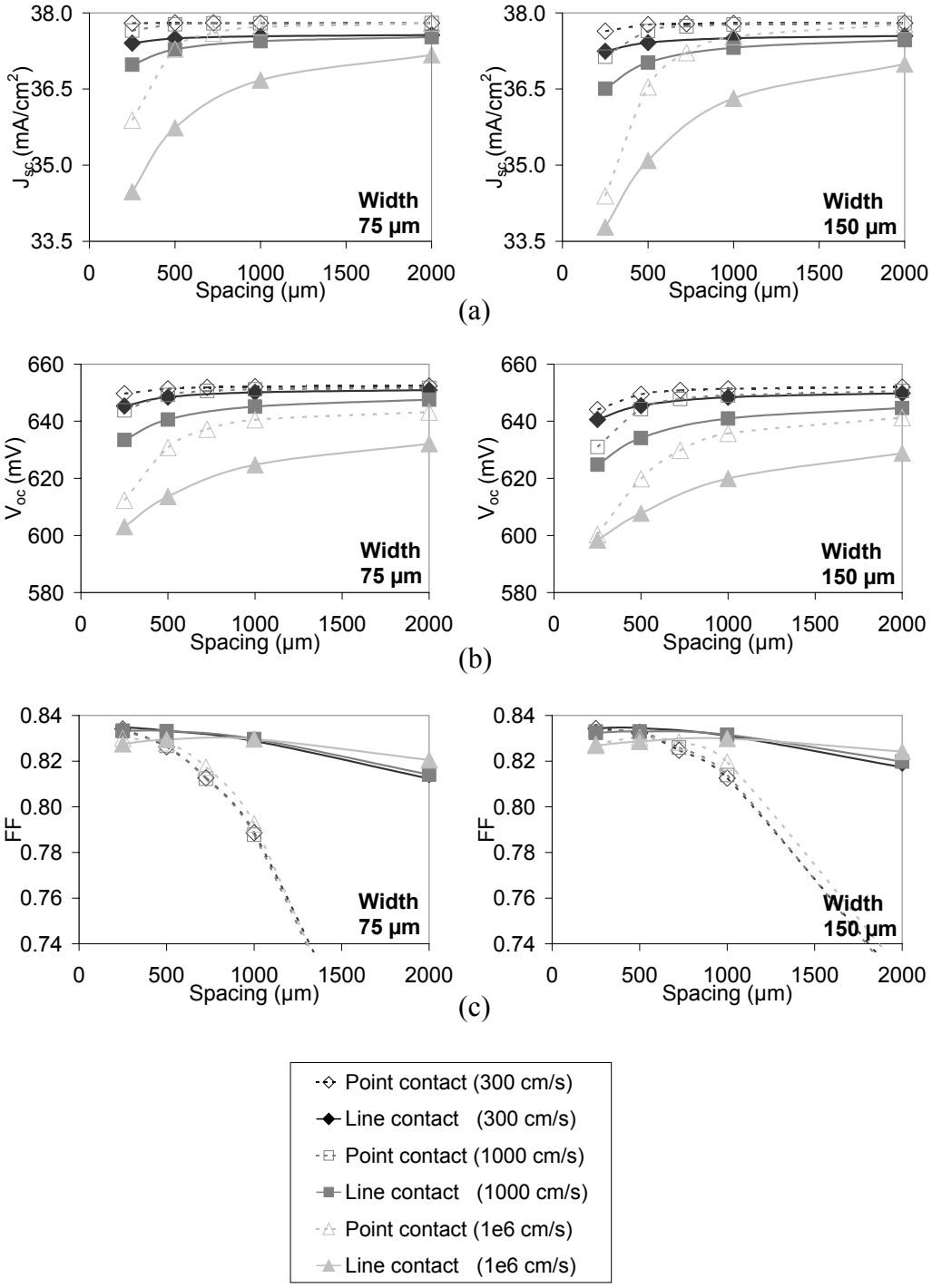


Figure 7.4 Simulated (a) J_{sc}, (b) V_{oc}, and (c) FF for the line and the point contact structures for contact widths of 75 and 150 µm and contact recombination velocities of 300, 1,000, 10^6 cm/s on 2.0 ohm-cm substrates.

As can be seen from Figure 7.3, the optimal spacing is a function of all the other contact variables considered: the contact geometry, the contact width, and the contact recombination velocity. Some of the key observations from these simulations are as follows:

- The optimal spacing is smaller for the point contact than for the line contact for the same contact width
- The optimal spacing is smaller for a smaller contact width for both the point and the line contact
- The optimal spacing is larger when the effective contact recombination is higher

The presence of the optimal spacing is the result of a competition between the resistive loss and the contact recombination loss. Increasing the spacing increases the resistive loss but decreases the impact of the contact recombination.

As mentioned above, the optimal spacing is smaller for the point contact than for the line contact. In addition, the optimum is sharper and more sensitive to the spacing for the point contact because the increase in the spacing increases the resistive loss much more rapidly compared to the line contact (as can be seen by a rapid drop in the FF with increasing spacing for the point contact design).

Cell efficiency of the point contact design at the optimal spacing is generally higher than that of the line contact design. However, for a low contact recombination velocity (~300 cm/s on 2.0 ohm-cm substrates in this case), both the geometries give similar efficiency at the optimal spacing.

In conclusion, the point contact can provide higher achievable efficiency but the spacing needs to be designed more precisely than the line contact. On the other hand,

reducing the recombination at the back contact by a high-quality LBSF allows the line contact design to achieve comparable efficiency to the point contact design.

7.1.3 Understanding the Effect of the Recombination at the Local Back Contact

To demonstrate the effect of the recombination at the back contact, efficiency of solar cells at optimal spacing for base resistivity of 2.0 ohm-cm was calculated and plotted as a function of contact recombination velocities, shown in Figure 7.5. It is clear from the figure that cell efficiency is a strong function of the contact recombination velocity. Also note that, for a given contact recombination velocity, the point contact design generally outperforms the line contact design. However, as mentioned above, the difference in cell performance between the two configurations becomes smaller when the SRV at the contact becomes small (≤ 300 cm/s on 2.0 ohm-cm substrates).

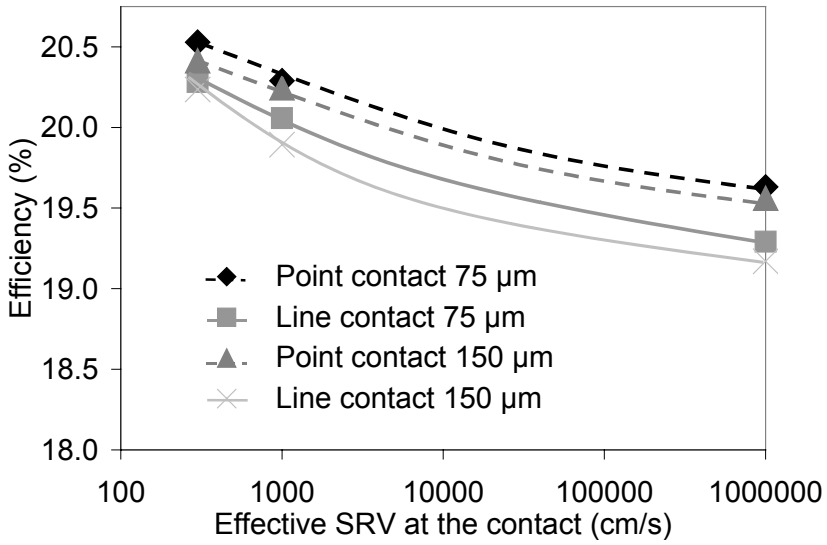


Figure 7.5 Simulated solar cell efficiency at optimal spacing as a function of contact recombination velocities for the point and the line back contact structures on 2.0 ohm-cm substrates.

7.1.4 Understanding the Effect of the Base Resistivity

Figure 7.6 shows simulated solar cell efficiency at optimal spacing as a function of base resistivity and SRV values at the contact for contact widths of 75 and 150 µm, for the point and the line back contact geometries. Their corresponding optimal spacing values are shown in Figure 7.7.

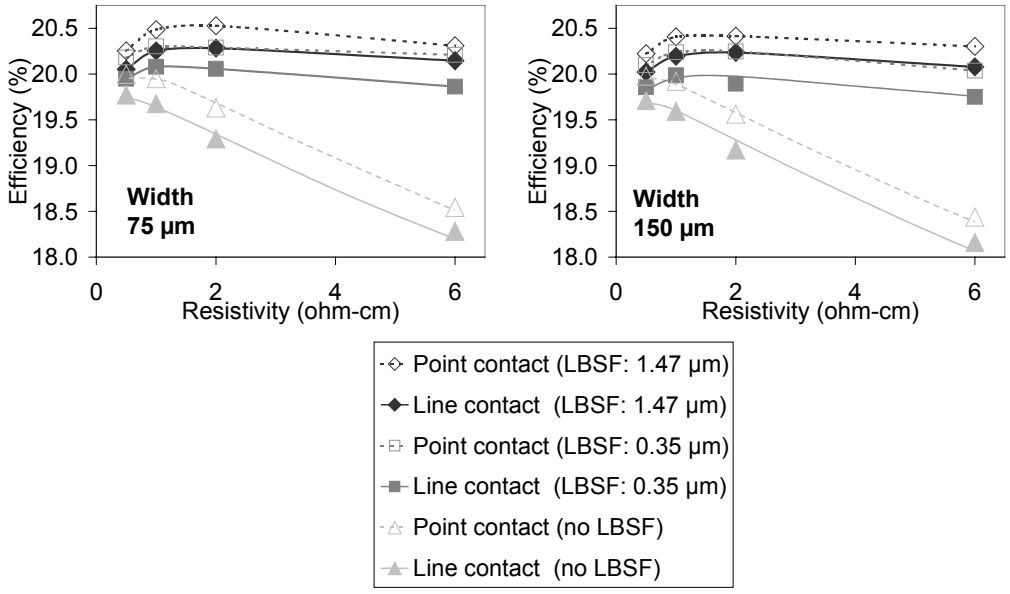


Figure 7.6 Simulated solar cell efficiency at optimal spacing as a function of the base resistivity for the line and the point contact structures for contact widths of 75 and 150 µm and varying LBSF thicknesses of 1.47, 0.35, and 0 µm (constant doping of 1×10^{19} cm^{-3}).

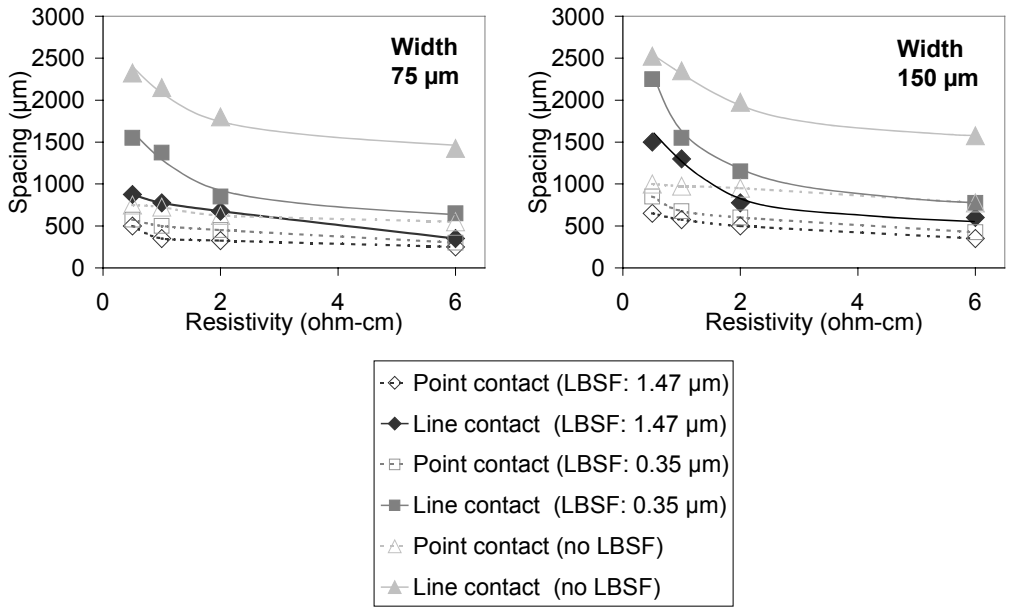


Figure 7.7 Optimal spacing as a function of the base resistivity for the line and the point contact structures for contact widths of 75 and 150 µm and varying LBSF thicknesses of 1.47, 0.35, and 0 µm (constant doping of 1×10^{19} cm^{-3}).

Some of the key observations from these simulations are as follows:

- The efficiency stays relatively independent of the base resistivity for cells *with* a LBSF (of at least 0.35 µm thick and constant doping of 1×10^{19} cm^{-3}).
- The efficiency becomes a strong function of the base resistivity for cells *without* a LBSF, where the efficiency drops linearly with increased resistivity.
- For the point contact geometry (with a contact with of ≤ 150 µm), the optimal spacing is always ≤ 1,000 µm. On the other hand, the optimal spacing for the line contact geometry can be up to ~2,500 µm.
- Optimal spacing decreases with increased resistivity

The simulations reveal that the formation of a LBSF becomes even more crucial for obtaining high-efficiency dielectric back-passivated cells on high-resistivity substrates. Additionally, when a LBSF is introduced, performance of the dielectric back-passivated cells becomes relatively independent of the base resistivity.

7.1.5 Understanding the Effect of the Lateral BSF around the Back Contact

All the simulations in the previous sections (Sections 7.1.2-7.1.4) were performed with a lateral BSF around the contact (Figure 7.8a). To investigate the impact of the lateral BSF on cell performance, additional simulations were performed without a lateral BSF (Figure 7.8b) for 75 μm and 150 μm contact widths with a LBSF thickness of 1.47 μm (constant doping of 1×10^{19} cm^{-3}) for both the line and point contact geometries on 2.0 ohm-cm substrates. Efficiency as a function of spacing for cells with and without a lateral BSF at the back contact is plotted in Figure 7.9.

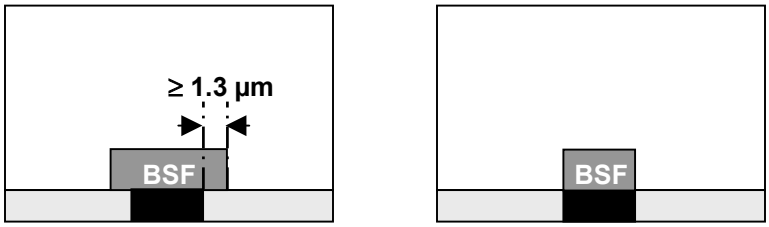


Figure 7.8 Schematic representation of a LBSF (a) with and (b) without a lateral BSF.

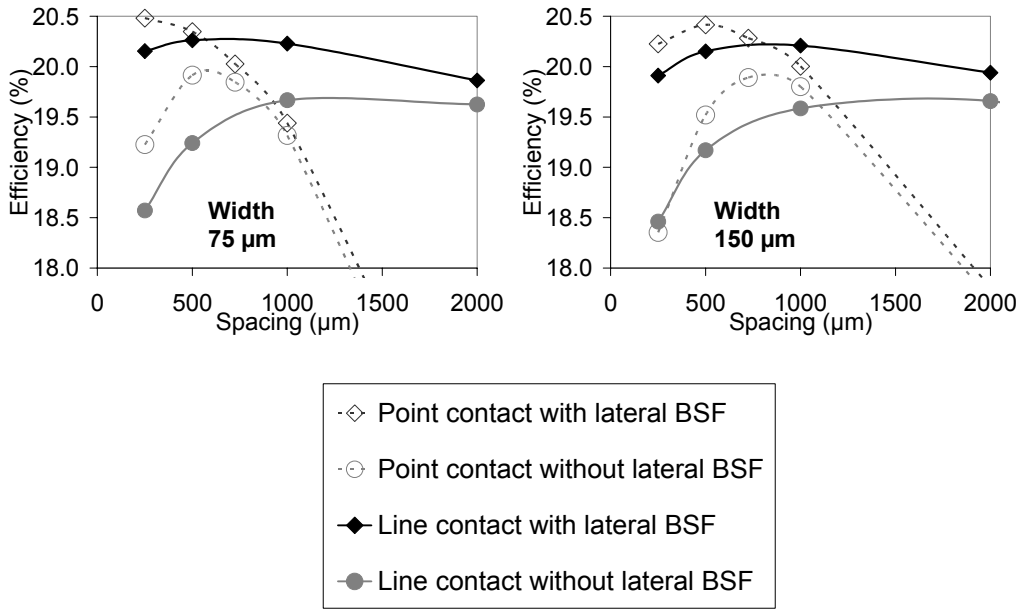


Figure 7.9 Simulated solar cell efficiency for the line and the point contact structures for contact widths of 75 and 150 µm and a LBSF thickness of 1.47 µm (constant doping of 1×10^{19} cm^{-3}) with and without a lateral BSF around the back contact on 2.0 ohm-cm substrates.

Figure 7.9 shows that the lateral BSF has a significant impact on cell performance as well as the optimal spacing design. For example, in the case of the point contact with a contact width of 150 µm on 2.0 ohm-cm substrates, the optimal efficiency reduces from 20.4% to 19.9% in the absence of the lateral BSF, while the optimal spacing increases from 500 µm to 800 µm.

These simulations reveal the importance of having a lateral BSF to achieve high cell performance. In the absence of the lateral BSF, the high recombination at the edge of the back contact is not suppressed and can greatly enhance the overall recombination at the back contact. The simulations also suggest that, to obtain the optimal design of the back contact by device modeling, the presence or absence of the lateral BSF should also be taken into account.

7.2 Device Simulations to Understand the Effect of Charge in the Back Dielectric Layer on LBSF Solar Cell Performance

PECVD SiN_x is a low-cost dielectric layer, which is widely used on the front surface of Si solar cells for anti-reflection and emitter passivation. Unfortunately, it does not do an adequate job of back surface passivation for LBSF cells. As mentioned in Chapter 3, the main drawback of PECVD SiN_x for back surface passivation of p-type Si solar cells is local back contact shunting of the inversion layer induced by the high positive charge density in SiN_x. In this section, the effect of charge in the dielectric on solar cell performance is investigated through 2-D simulations.

7.2.1 Overview of the 2-D Device Simulation to Understand the Effect of Charge in the Back Dielectric Layer

The unit device structure used to simulate the effect of charge in the back dielectric layer is shown in Figure 7.10. It consisted of a local back contact, formed through a dielectric layer with a 75-μm line width and 1000 μm spacing. A thin (20 nm) heavily B-doped (1×10^{21} cm^{-3}) p^+ Si layer was introduced underneath the local contact to create an ohmic back contact via tunneling. The tunneling mechanism [124-126] allows an ohmic contact to be formed onto heavily doped p^+ Si with a wide variety of metal work function. As will be shown in the next section, during the simulation, the shunt path between the back contact and the inversion layer (formed by positive charge in the dielectric) could be turned on or off by altering work function of the metal back contact.

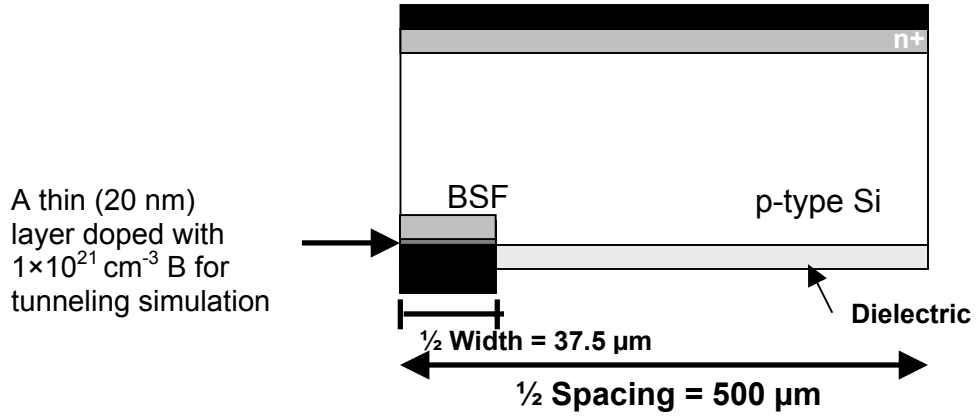


Figure 7.10 Simulation domain used in the investigation of the effect of charge in the back dielectric of a p-type Si solar cell. A thin (20-nm thick) heavily doped (1×10^{21} cm^{-3}) layer is introduced to simulate the tunneling ohmic contact with a low work function metal on p-type Si.

The fixed material and device parameters used for the simulations are shown in Table 7-3. The S_{n0} and S_{p0} values of 1,000 and 15 cm/s were taken from [127], where they were used to simulate the recombination activity at the Si-SiO_2 interface. These values are used here to demonstrate the impact of asymmetrical capture cross-section of defects at the dielectric/Si interface.

Table 7-3 Fixed parameters used in the investigation of inversion shunting.

Parameters	Values
Emitter sheet resistance	80 ohm/sq (Gaussian profile with a surface concentration of 1.139×10^{20} cm^{-3} and a junction depth of 0.3 μm)
Cell thickness	200 μm
Resistivity	2.0 ohm-cm (unless mentioned otherwise)
SRH lifetime (midgap traps: $E_t=0$) $\tau_{n0}=\tau_{p0}$	1,000 μs
Front SRV	60,000 cm/s
BSRV at dielectric	S_{n0} =1000 cm/s S_{p0} = 15 cm/s With midgap trap ($E_t=0$)
Optical generation	Textured (facet angle = 54.74°), 8.5% shading, with SiN_x (750 Å, n=2) R_{front} (internal)=0.92 R_{back} (internal)=0.85
Contact resistance	0 ohm-cm^2
Contact formation	Line contact (2-D), 75-μm width, 1000-μm spacing, and a 1.47-μm thick (1×10^{19} cm^{-3}) BSF coupled with a 20-nm thick (1×10^{21} cm^{-3}) layer as shown in Figure 7.10

7.2.2 Simulation of Shunting Between the Inversion Layer and the Back Contact by Altering Work Function of the Metal Back Contact

Using the cell structure in Figure 7.10, cell efficiency as a function of work function of the metal back contact was simulated for dielectric with and without a charge density of $+2.5\times10^{12}$ cm^{-2} (shown in Figure 7.11). Without the dielectric charge, work function has negligible impact on cell efficiency, which confirms that the tunneling contact in Figure 7.10 is capable of forming ohmic contact for all metal work function values used in these simulations. However, when the dielectric contains a positive charge density of 2.5×10^{12} cm^{-2}, there exists a threshold value of metal work function, below which the cell efficiency drops noticeably. As explained below, this drop in the efficiency is a result of an electrical shunt path between the dielectric induced inversion layer and the low work

function back metal contact (<5 eV), which induced an inversion layer underneath the contact. A low work function metal is able to invert the p^+ region underneath it and the two inversion layers get shunted. The objective of this section is to explain how a shunt path is formed in the simulation when a low work function metal is used. It should be recognized, however, that this structure is solely used as a tool to allow a simulation of a shunt path in the device and is not intended to represent the mechanism responsible for parasitic shunting in actual devices.

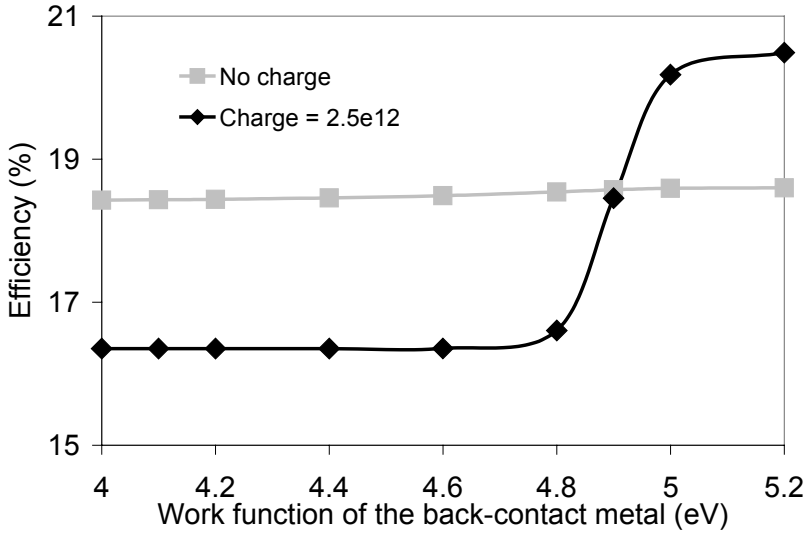


Figure 7.11 Simulated solar cell efficiency as a function of work function of the back contact for dielectric with and without charge of 2.5×10^{12} cm^{-2}.

To understand how the shunt path can be controlled by altering work function of the metal back contact, it is instructive to consider the Si energy band diagram at the back surface in the vicinities of the dielectric and the metal back contact shown in Figure 7.12 and Figure 7.13, respectively. At thermal equilibrium, the electric field induced by positive charge in the dielectric creates an inversion layer or a p-n junction in the Si underneath (as seen by the band bending to lower energy in Figure 7.12a). As light starts to inject carriers into the cell, the p-n junction between the inversion layer and the p-type

Si bulk becomes forward bias, resulting in reduction of the band bending as shown in Figure 7.12b. In fact, light-induced forward bias of the junction is responsible for this type of surface passivation because it re-injects the light generated minority-carrier electrons back into the base to maintain the charge neutrality in the vicinity of the Si surface and the dielectric. The rate of electrons injected (loss) into this junction from the base is limited by the rate of recombination in the inversion layer and at the Si surface. This, however, is only true when the junction is kept floating and no shunt path is present.

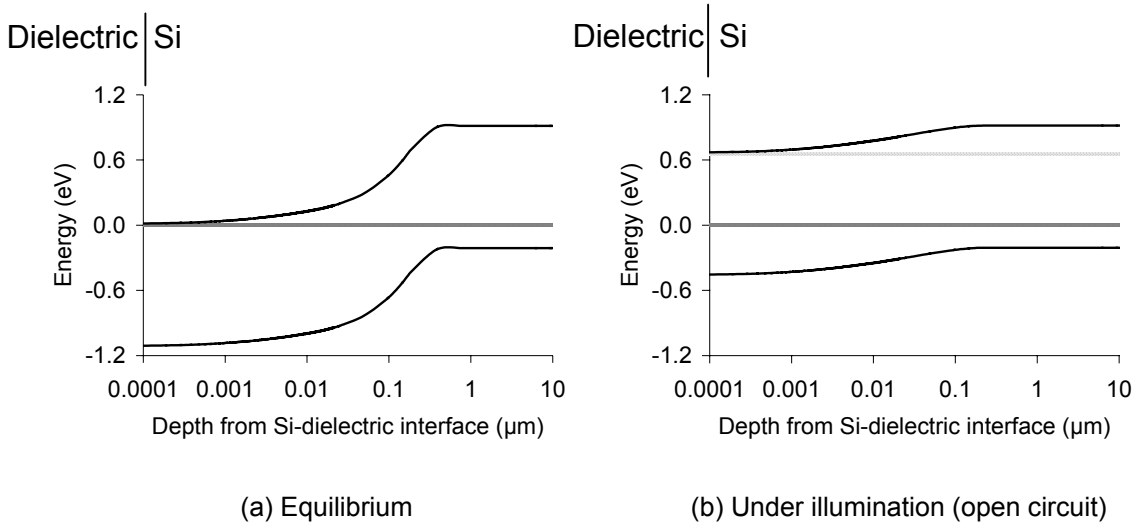
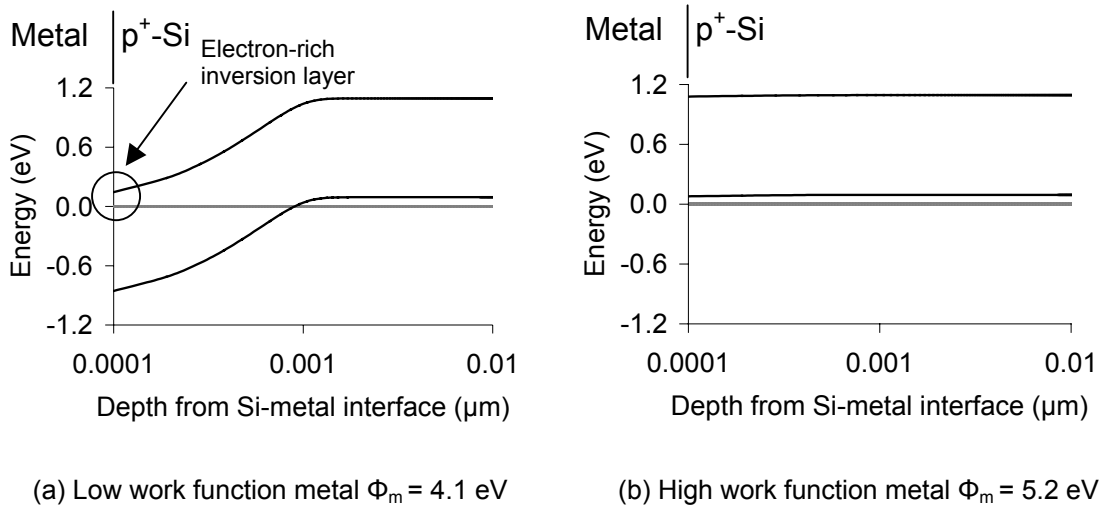


Figure 7.12 Energy band diagram of Si as a function of distance from the dielectric/Si interface under (a) equilibrium and (b) illumination at an open-circuit condition. The charge density in the dielectric layer was fixed at 2.5×10^{12} cm^{-2}. Note that a logarithm scale is used for the x-axis.



(a) Low work function metal Φ_m = 4.1 eV (b) High work function metal Φ_m = 5.2 eV

Figure 7.13 Energy band diagram of Si under equilibrium as a function of distance from the metal/Si interface for metal work function of (a) 4.1 eV and (b) 5.2 eV. Note that a logarithm scale is used to clearly show the band bending, which occurs only in the first 1 nm from the interface for this heavily doped Si (1×10^{21} cm^{-3}).

Depending upon work function of the metal used in the simulation, the band bending of p^+-Si underneath the contact can vary: a lower work function metal tends to create inversion in the p^+-type Si (Figure 7.13a), while a higher work function metal tends to create a flat band condition or accumulation in the p^+ Si (Figure 7.13b). These two very different behaviors allow us to turn on and off the shunt path in the simulation. The low work function metal creates an inversion layer underneath its such that there is a conduction path for electrons present in the dielectric-induced inversion layer to flow to the inversion layer created by the metal back contact. This allows the electrons in the dielectric inversion layer to leak or shunt to the back contact. Consequently, the inversion layer p-n junction (by the dielectric) is not able to become forward bias (to re-inject the electrons back into the base). As a result, the electrons that flow to this junction are

directly sent to the contact where they recombine with holes. On the other hand, the high work function metal does not create band bending or inversion underneath, resulting in energy potential to prevent electrons in the dielectric-induced inversion layer from flowing to the contact. The inversion layer p-n junction is therefore floating and is able to become forward bias.

7.2.3 Effect of Charge Property and Density in the Back Dielectric on LBSF Solar Cell Performance

Effect of charge in the back dielectric on LBSF cell performance is discussed in this section. First subsection focuses on the dielectric that contains different amount of a positive charge density. In this case, the simulation was performed both with and without the inversion shunting by using low (4.1 eV) and high (5.2 eV) work function metals, respectively. The second subsection focuses on dielectric that contains a different amount of a negative charge density. In this case, only a low work function metal of 4.1 eV is used in the simulation, as there is no concern on shunting.

7.2.3.1 Effect of the Positive Charge Density on the Performance of LBSF Cells

This section is divided into two parts. The first part explains in detail the observed trend of efficiency as a function of the positive charge density in the back dielectric. Here, the case of 2.0 ohm-cm substrates is considered as an example. Subsequently, in the second part, simulation results extended to cover other base resistivity are presented.

7.2.3.1.1 Understanding the Effect of the Positive Charge Density on Performance of LBSF Cells

Figure 7.14 shows simulated solar cell efficiency as a function of the amount of the positive charge density in the back dielectric with and without a parasitic shunt path for

2.0 ohm-cm substrates. As explained in the previous section, shunt was turned on and off simply by using low (4.1 eV) and high (5.2 eV) metal work function, respectively. Also included in the figure are two dash-dotted lines representing the efficiency of LBSF cells with no dielectric charge and two extremes of surface recombination velocities of 0 cm/s (no recombination) and 1×10^6 cm/s (as high recombination as the metal/Si interface).

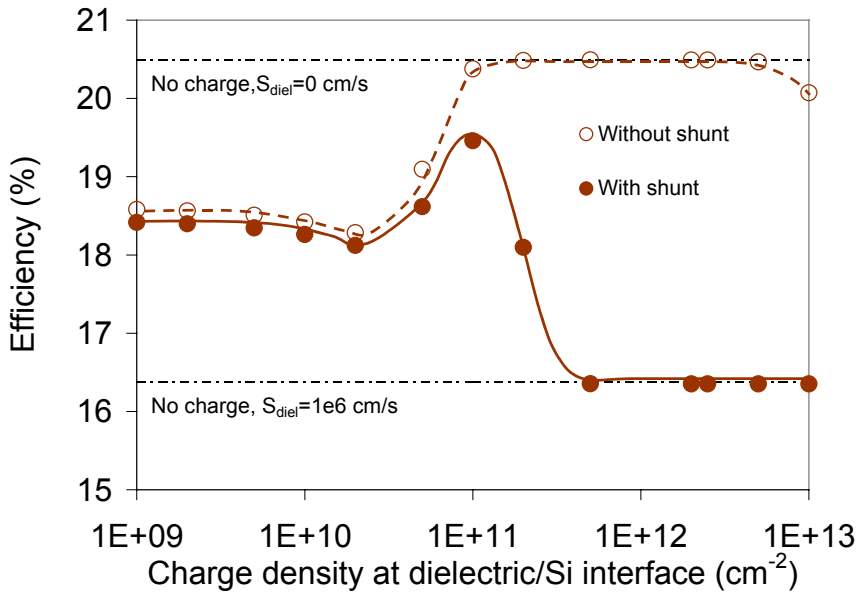


Figure 7.14 Simulated efficiency of a 2 ohm-cm p-type Si cell as a function of the positive charge density in the back dielectric with and without a shunt path to the back contact. Dash-dotted lines represent two extreme cases of zero-charge dielectric with surface recombination velocities of 0 and 10^6 cm/s.

To understand the efficiency trend in Figure 7.14, the curve with no shunt path will be considered first. In this case, the trend of efficiency as a function of dielectric charge can be solely explained by the charge-induced change in the effective SRV at the Si/dielectric interface. The effective SRV is a function of (1) n_s (cm^{-3}) and p_s (cm^{-3}), which represent the electron and the hole concentrations at the Si/dielectric interface, (2) S_{n0} and S_{p0}, which are the characteristic recombination velocities of electrons and holes at the Si/dielectric interface, and (3) Δn (cm^{-3}), which is the injection level in the Si bulk

near the surface. The SRV can be divided into four main regimes based on the amount of positive charge in the dielectric:

(a) Effective SRV = S_{n0} for a very small positive charge density (<2×10^{9} cm^{-2}).

Low amount of charge has no impact on the carrier concentration at the surface. Therefore, the surface remains hole abundant (p-type) in this regime. Here, the effective SRV is dictated by the capturing rate of electrons, which stays constant and equals to S_{n0}. Hence, the efficiency is independent of the charge density in this regime.

(b) Effective SRV=$\frac{1}{\Delta n}\frac{n_s p_s (S_{p0}\cdot S_{p0})}{S_{n0}n_s + S_{p0}p_s}$ for a low positive charge density (2×10^{9} cm^{-2}<charge<2×10^{10} cm^{-2}).

The amount of charge is now sufficient to attract electrons to the surface such that the electron concentration becomes comparable to the hole concentration at the surface. Nevertheless, the charge in this regime is still insufficient to create an inversion condition. With increasing charge in this regime, the recombination rate increases because more electrons are available for recombining with holes at the surface. Hence, efficiency drops with increasing charge until the minimum efficiency is reached, where the combination of electron and hole concentrations at the surface becomes most favorable for recombination (i.e., $S_{no}n_s=S_{p0}p_s$ for midgap traps). This corresponds to a charge density of 2×10^{10} cm^{-2} in this scenario.

(c) Effective SRV $=\frac{p_s}{\Delta n}\cdot S_{p0}$ for a moderate positive charge density (2×10^{10} cm^{-2} <charge<2×10^{11} cm^{-2}).

The amount of charge becomes sufficiently high that it induces an inversion condition resulting in abundant electrons but limited holes at the surface. Here, the effective SRV is dictated by the capturing rate of holes. Increasing charge in this regime causes holes at

the surface to become less available, which then limits the recombination even further. Hence, the efficiency increases with increasing positive charge in this regime.

(d) Effective SRV = 0 cm/s for a high positive charge density (>2×10^{11} cm^{-2}).

In this regime, the positive charge density is sufficiently high that it induces a strong inversion condition, where holes at the surface (p_s) becomes much smaller than Δn. Consequently, the effective SRV stays constant with the SRV value closed to 0 cm/s. Hence, the efficiency stays very high and independent of the charge density in this regime. This is how a floating junction with no shunting works very effectively in Figure 7.14.

The effect of the positive charge density on the efficiency changes when a contact induced shunt path is present, and the inversion layer junction is no longer floating. For the charge density below 1×10^{11} cm^{-2}, the efficiency trend is similar to the case without a shunt path and is governed by the dielectric SRV. As charge increases beyond 1×10^{11} cm^{-2}, the efficiency, instead of increasing, drops to a very low value of 16.4%, which is even lower than the initial value of 18.6%. As explained in the previous section, in this case, the inversion layer behaves as a conduit to transport the collected electrons from the bulk to recombine at the contact, instead of re-injecting them back into the bulk. In fact, the effective surface recombination becomes as high as 1×10^{6} cm/s (Figure 7.14). Thus, dielectric passivation with high positive charge can actually degrade cell performance in the presence of a shunt and the device could become much worse than a regular Al-BSF cell.

7.2.3.1.2 Understanding the Impact of the Base Resistivity on Performance of LBSF Cells with Positively Charged Dielectric

Additional simulations were performed to investigate the impact of the base resistivity on the performance of LBSF cells with positively charged dielectric. The resistivity included in these simulations are 0.5, 1.0, 2.0, and 6.0 ohm-cm. Note that all other parameters were kept the same as in Table 7-3.

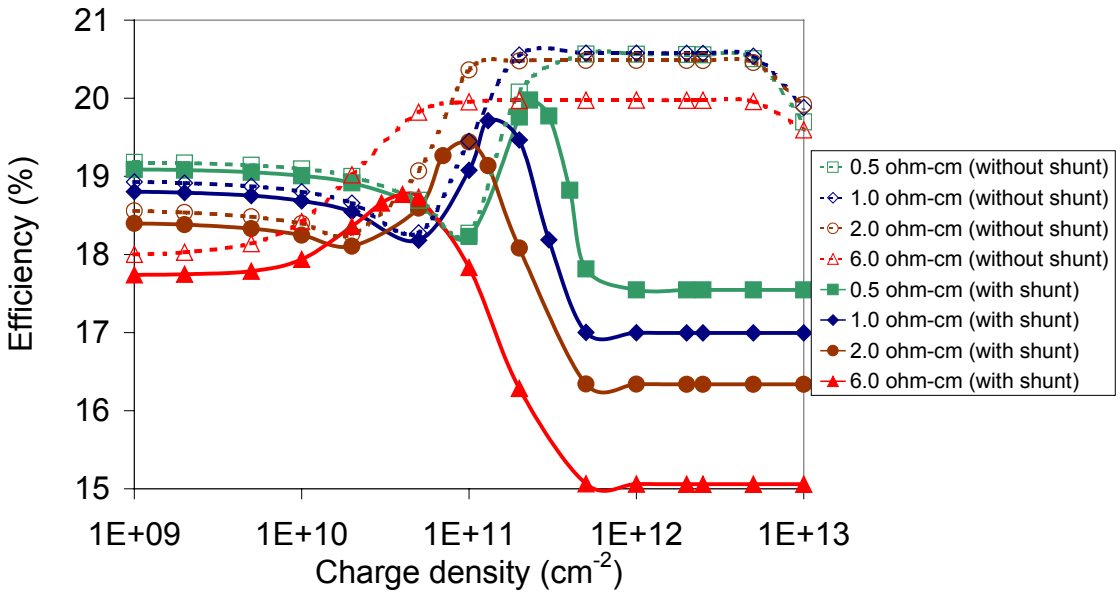


Figure 7.15 Simulated efficiency of p-type Si cells as a function of the positive charge density in the back dielectric for different base resistivity of 0.5, 1.0, 2.0, and 6.0 ohm-cm, with and without a shunt path to the back contact.

Figure 7.15 shows the simulated solar cell efficiency as a function of the amount of the positive charge density in the back dielectric for base resistivity of 0.5, 1.0, 2.0, and 6.0 ohm-cm, with and without a parasitic shunt path. The trends of efficiency as a function of the positive charge density are very similar for all the base resistivity. The main difference lies in the amount of charge densities where different regimes take place. The efficiency trend shifts toward lower charge densities with increasing base resistivity

because substrates with lower doping are easier to be affected by charge in the dielectric. Consequently, the optimal charge density that gives the highest efficiency for the cells with a parasitic shunt path becomes lower for higher base resistivity. The optimal positive charge densities were found to be 2.5×10^{11}, 1.5×10^{11}, 1.0×10^{11}, and 4.0×10^{10} cm^{-2} for the base resistivity of 0.5, 1.0, 2.0, and 6.0 ohm-cm, respectively. Note that this is applicable to the cells with a *severe* parasitic shunt path between the inversion layer and the back contact

7.2.3.2 Effect of the Negative Charge Density on the Performance of LBSF Cells

Similar to the case of the positive charge density, this section is divided into two parts. The first part deals with the explanation of the trend of efficiency as a function of the negative charge density in the back dielectric for 2.0 ohm-cm substrates. Simulation results extended to other base resistivity are then presented in the second part.

7.2.3.2.1 Understanding the Effect of the Negative Charge Density on Performance of LBSF Cells

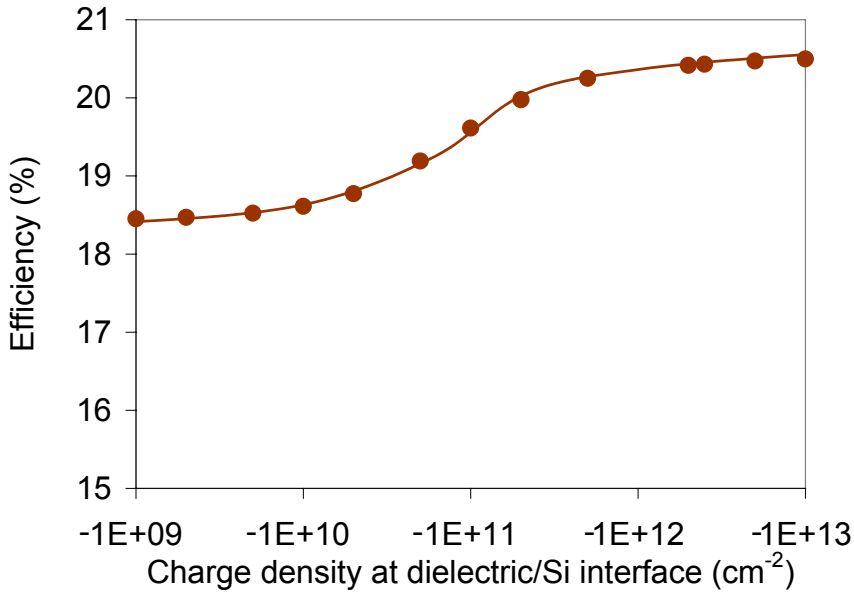


Figure 7.16 Simulated efficiency of a 2 ohm-cm p-type Si cell as a function of the negative charge density in the back dielectric.

Figure 7.16 shows simulated cell efficiency as a function of the negative charge density in the back dielectric for 2.0 ohm-cm substrates. In this case, the trend of efficiency as a function of the dielectric charge density can solely be explained by the change in the effective SRV at the Si/dielectric interface. The SRV can be divided into three main regimes with respect to the negative charge density in the dielectric:

(a) Effective SRV = S_{n0} for a very small negative charge density ($|\text{charge}| < 2\times10^{9}$ cm^{-2}).

Low amount of charge has no impact on the carrier concentration at the surface. Therefore, the surface remains hole abundant (p-type) in this regime. Here, the effective SRV is dictated by the capturing rate of electrons, which stays constant and equals to S_{n0}. Hence, the efficiency is independent of the charge density in this regime.

(b) Effective SRV $= \frac{n_s}{\Delta n} \cdot S_{n0}$ for a moderate negative charge density (2×10^{9} cm^{-2}<$|\text{charge}|$<1×10^{12} cm^{-2})

The amount of charge becomes sufficiently high that it induces an accumulation condition, which further limits the number of electrons at the surface. Here, the effective SRV is dictated by the capturing rate of electrons. Increasing charge in this regime causes electrons at the surface to become less available, which then limits the recombination even further. Hence, the efficiency increases with increasing negative charge in this regime.

(c) Effective SRV = 0 cm/s for a high negative charge density ($|\text{charge}|>1\times10^{12}$ cm^{-2}).

In this regime, the negative charge density is sufficiently high that it induces a strong accumulation condition, where electrons at the surface (n_s) becomes much smaller than Δn. Consequently, the effective SRV stays constant with the SRV value closed to 0 cm/s. Hence, the efficiency stays very high and independent of the charge density in this regime.

These simulations suggest that negatively charged dielectric is very desirable because it not only provides excellent passivation but also prevents back contact shunting. Although negatively charged dielectric layers are not as common as positively charged ones, some researchers have demonstrated selected dielectric layers with negative charge. This is discussed briefly in Section 7.3.

7.2.3.2.2 Understanding the Impact of the Base Resistivity on Performance of LBSF Cells with Negatively Charged Dielectric

Additional simulations were performed to investigate the effect of the base resistivity on performance of LBSF cells with negatively charged dielectric. The resistivity values used in these simulations are 0.5, 1.0, 2.0, and 6.0 ohm-cm. All other parameters were kept the same as in Table 7-3.

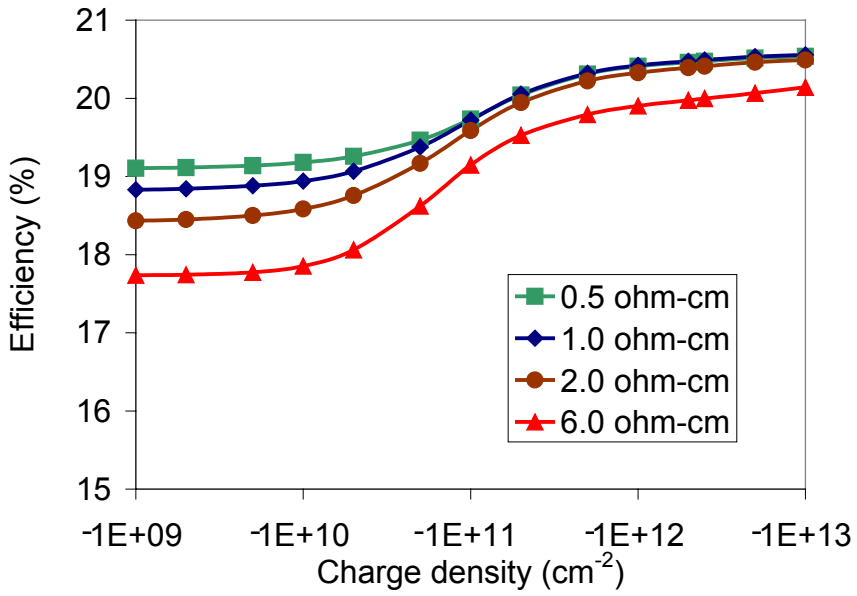


Figure 7.17 Simulated efficiency of p-type Si cells as a function of the negative charge density in the back dielectric for different base resistivity of 0.5, 1.0, 2.0, and 6.0 ohm-cm.

Figure 7.17 shows the simulated solar cell efficiency as a function of the amount of the negative charge density in the back dielectric for base resistivity of 0.5, 1.0, 2.0, and 6.0 ohm-cm. The efficiency trend as a function of the negative charge density in the back dielectric for all resistivity shows the same general appearance. Similar to the positive charge case, the difference lies in the amount of charge densities where different regimes take place. The trend of efficiency as a function of the charge density shifted toward lower charge densities with increasing base resistivity. Nevertheless, the same conclusion

holds for all resistivity values where the simulations suggest that higher amount of negative charge leads to better cell performance.

7.3 Proposed Structure and Process Scheme for Low-Cost Dielectric Back-Passivated p-Type Si Solar Cells

Figure 7.18 provides an overview of possible structures to address the contact recombination, the surface recombination, and the shunt path issues in dielectric back-passivated p-type Si solar cells.

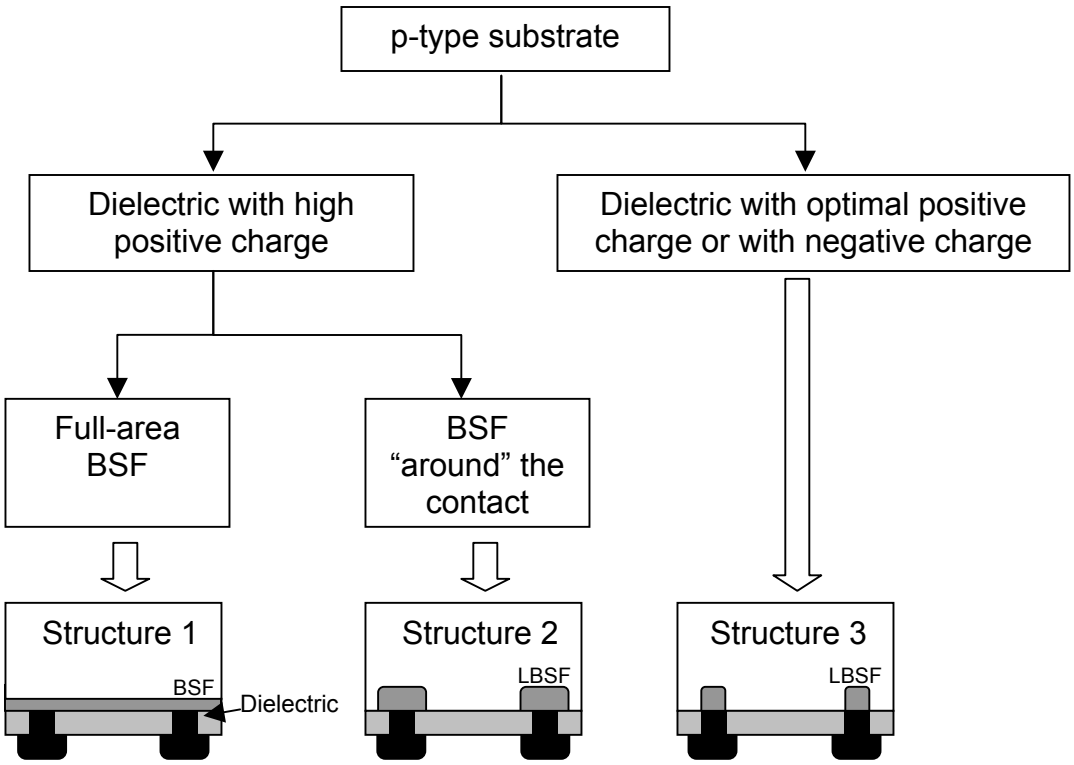


Figure 7.18 Structures for high-efficiency dielectric back-passivated solar cells.

Structures 1 and 2 can readily be achieved by employing PECVD SiN_x as a passivation layer. In both structures, a heavily p-type doping concentration at the surface can prevent the formation of an inversion layer and, hence, eliminate the shunting issue. However, both the structures require additional p-type diffusion rather than self-doping

by the Al contact. This is normally achieved by B-diffusion. Diffusion of B raises a concern of introducing another process step as well as the B-diffusion induced minority-carrier lifetime degradation in the bulk as discussed in Chapter 3. The B-diffusion process needs to be strictly controlled to preserve the lifetime through the diffusion process. Furthermore, in Structure 2, first, wider local B-BSF regions need to be diffused, and then local contacts need to be formed *inside* the B-diffused areas. Such a structure requires a masking and an aligning step, which results in a highly complicated process.

Structure 3 relies on the development of an appropriate dielectric layer with an optimal positive charge density or with a high negative charge density to eliminate the inversion-shunting by avoiding the formation of strong inversion underneath the dielectric. This structure has the highest potential for a high-throughput process since self-doping by Al can readily be used to form a LBSF without any additional process steps. Note that if there is a strong inversion layer underneath the dielectric then there could be shunting at the edge of the contact because the p^+ region may not completely decouple the contact and the inversion layer. Some dielectric layers have been proposed in the literature to provide an optimal positive charge including stacked thermal oxide/PECVD SiN_x and modified SiN_x. A study in [128] demonstrated that a single crystalline Al_2O_3 layer not only contained high negative charge but also exhibited excellent surface passivation on p-type Si substrates. However, the process of depositing crystalline Al_2O_3 is currently too complicated for a high production volume. A study on a spin-on source containing Al_2O_3 was also conducted in [128] but the layer exhibited a stability problem at that time.

Structure 3 will be explored in this thesis because it has the highest potential for implementation with a low-cost process. The dielectric will be based on spin-on technology in combination with PECVD SiN_x.

To achieve Structure 3, a process scheme compatible with screen-printing technology is proposed in Figure 7.19.

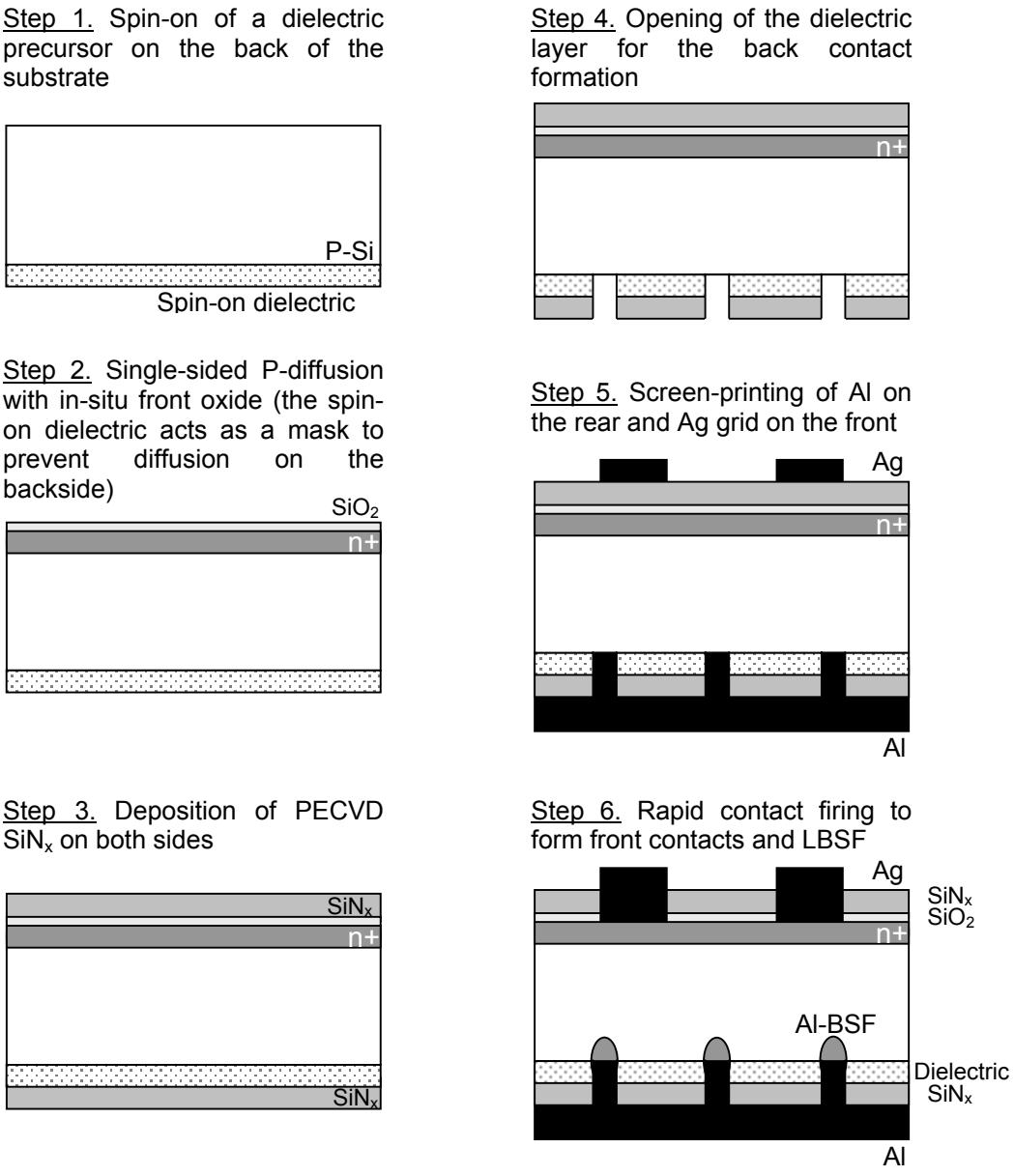


Figure 7.19 Proposed process to fabricate low-cost dielectric back-passivated solar cells.

7.4 Conclusions

Two and three dimensional device simulations were performed to understand the requirements and cell designs that can produce high performance dielectric back-passivated cells by a low-cost process. The first part of the study involved establishing the size and the spacing of the openings through the dielectric to achieve the best compromise between the resistance and the contact-induced recombination. The optimal spacing of the openings was found to be a function of several input parameters such as the size and the geometry of the opening, the base resistivity, and the contact recombination velocity. The key finding from these simulations was that, in addition to the need to form a LBSF at the openings for high efficiency, the presence or absence of a lateral BSF region around the openings plays an important role in dictating cell performance as well as the optimal spacing.

In the second part of the study, 2-D simulations were performed to investigate the effect of charge in the dielectric layer on performance of dielectric back-passivated p-type Si solar cells. First, a simulation technique was developed and incorporated into the Dessis program to simulate the effect of the inversion layer shunting as a function of the positive charge density in the back dielectric layer. Next, it was established that for p-type Si cells with a severe parasitic shunt path between the inversion layer and the back contact, the dielectric positive charge density should be kept at around 2.5×10^{11}, 1.5×10^{11}, 1.0×10^{11}, and 4.0×10^{10} cm^{-2} for the base resistivity of 0.5, 1.0, 2.0, and 6.0 ohm-cm, respectively. It was also found that, for p-type cells, negative charge in the back dielectric layer is more desirable and higher amount of negative charge leads to better cell performance.

Based on the above understanding from the simulations, a cell structure was established that has potential for achieving low-cost high-efficiency dielectric back-passivated p-type Si solar cells. This structure has two main requirements: (1) a back dielectric layer with high-quality surface passivation and either a moderate positive charge or a high negative charge density and (2) a low-cost LBSF formed by self-aligned Al-Si alloying. Next chapter deals with the experimental development of these two areas.

CHAPTER 8

DEVELOPMENT OF A METALLIZATION PROCESS AND A DIELECTRIC LAYER FOR LOW-COST DIELECTRIC BACK-PASSIVATED P-TYPE SI SOLAR CELLS

To fabricate low-cost screen-printed dielectric back-passivated p-type Si solar cells, proposed at the end of Chapter 7, two novel technology developments were carried out in this chapter. These include (1) development of a metallization technique that combines opening holes through the back dielectric and Al-paste screen-printing and firing to simultaneously form local contacts, a LBSF, and an internal back reflector and (2) development of a dielectric layer that not only provides high-quality surface passivation, but also contains either a moderate positive charge density or a high negative charge density to prevent the formation of a strong inversion layer. These two developments involved significant technology development and comprehensive characterizations and analysis of contacts, dielectric and cells described in the following sections.

8.1 Development of a Metallization Technique to Simultaneously Form Local Contacts in Conjunction with a LBSF and an Internal Back Surface Reflector

The proposed technology to achieve local contacts, a LBSF, and an internal back surface reflector involves the formation of local openings through a dielectric layer prior to full-area Al screen-printing and rapid firing (see Figure 8.1). Using the back dielectric layer as a mask, local contacts are made through the openings, while high-quality back surface passivation and high internal back surface reflectance are achieved in the region covered by the dielectric. Generally, local openings account for less than 5% of the back

surface while > 95% of the back surface is protected by dielectric. Additionally, the use of screen-printed Al forms a self-aligned LBSF underneath the local Al contact after firing. The LBSF between the metal and Si substrate is crucial for achieving good ohmic contact to a high resistivity substrate (>1 ohm-cm) and for minimizing the negative impact of high recombination at the metal/Si interface.

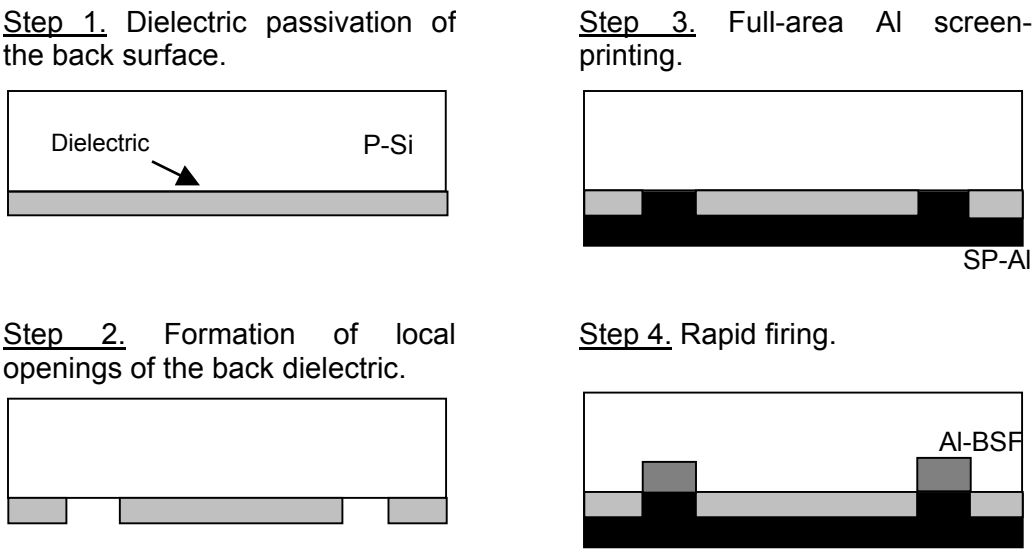


Figure 8.1 Schematic of a simple process to form local back contacts, a LBSF, and a back reflector.

It is very challenging to make this process work using low-cost technologies like screen-printing because (1) clean dielectric openings need to be formed at low cost, (2) appropriate dielectric needs to be used, (3) surface passivation needs to be maintained after contact firing, (4) high internal back surface reflection needs to be achieved at the metal-dielectric interface, and (5) a high-quality LBSF needs to be formed between the Al metal and the Si substrate.

In this study, LF-SiN_x was chosen as one of the key dielectric layers because it is a commercially established process, and it can serve as a mask for metal impurities from the paste.

This section describes the development of an Al paste to satisfy the above requirements to achieve high efficiency LBSF cells. Four Al pastes were investigated in this study: (1) *fritted* Al paste (regular Al paste with glass frit, which is commercially used for full-area Al-BSF structures), (2) *fritless* Al paste, (3) *fritless* Al paste with 7% Si, and (4) *fritless* Al paste with 12% Si. These four pastes were analyzed in terms of contacts, a LBSF, and a back reflector. Additionally, dielectric back-passivated cells with a LBSF were fabricated using these four pastes to assess their impact on cell performance. The experimental approach is discussed in detail below.

The impact of firing and the Al paste composition on the surface passivation quality was studied by first growing thin thermal SiO_2 (~100 Å) on a 2.4 ohm-cm FZ Si sample at 875°C in a conventional tube furnace. LF-SiN_x with a thickness of ~650 Å was then deposited on both sides of the samples (on top of the SiO_2 layers). Subsequently, each of the four Al pastes were screen-printed on one side of each sample followed by 750°C/3s firing in a belt furnace. Samples without Al printing were also included in the firing as references. After the firing, all samples were placed in an $HCl:H_2O_2:H_2O$ (1:1:2 by volume) solution to remove the Al layer without removing the dielectric layer. Finally, the effective lifetime was measured by the photoconductance decay method at an excess carrier concentration of 2×10^{14} cm^{-3}, which was used as an indicator of the surface passivation quality after Al firing.

The impact of the Al paste composition on the internal back surface reflectance was examined by depositing ~1,000 Å of a SiN_x film on both sides of FZ Si samples. The four Al pastes were then screen-printed on the backside. A sample with SiN_x only on the front and fritted Al on the back was also prepared to represent the conventional Al-BSF

structure. All samples were fired in a belt furnace using the same firing condition (750°C/3s). Finally, total reflectance was measured from the front side of the samples. An increase in the escape reflectance at wavelength of > 1,000 nm was used as an indicator of the back surface reflectance and was used to extract the internal back surface reflectance value.

To examine the impact of the Al paste composition on the quality of the LBSF formation, test structures were prepared according to the process scheme shown in Figure 8.1. The openings were formed by (1) screen-printing of a SolarEtch paste from Merck KGaA (an HF-free paste containing a special PO_4^{3-} complex for SiO_2 and/or SiN_x selective etching) with an on-screen design of 125×125 μm^2 square openings, (2) annealing at 350°C for 30s to initiate the etching reaction, and (3) rinsing in deionized water to remove the etching residue. Subsequently, the four Al pastes were screen-printed on the samples. The samples were then fired in a belt furnace. Cross-sections of all four samples were prepared for an SEM analysis by sectioning through the openings followed by polishing and etching to delineate the p-p^+ region. This allowed examination of the uniformity and depth of the LBSF under the contacts. A deep and uniform BSF layer indicates a good BSF formation.

Finally, 4 cm^2 screen-printed dielectric back-passivated solar cells were fabricated. First, a 45 ohm/sq emitter was formed by $POCl_3$ diffusion followed by back side Si etching to remove an n^+ layer from the back surface, where a SiN_x layer was used to protect the front surface. The samples were then oxidized at 875°C to obtain 150-200 Å thick SiO_2 on the front emitter and 80-100 Å thick SiO_2 on the back. Subsequently, LF-SiN_x with a thickness of 600-700 Å was deposited on both sides of the samples. Local

openings through the back dielectric were formed using the solar etch paste from Merck described above. Samples were subjected to full-area screen-printing of the four Al pastes on the backside, followed by Ag-gridline printing on the front side. The samples were then fired in a belt furnace to form front and back contacts, a LBSF, and a back reflector. Finally, an FGA at 400°C was performed to ensure good ohmic contact. The finished cells were analyzed by light I-V and LBIC-response measurements.

8.1.1 Effect of the Al Composition and Firing on the Passivation Quality of SiO_2/SiN_x

Effective lifetimes measured on SiO_2/SiN_x passivated samples after firing with the four different Al pastes on top of the dielectric are shown in Figure 8.2. Figure 8.2 also shows the effective lifetime of a sample fired with no Al printing. It was found that 2.4 ohm-cm FZ samples with SiO_2/SiN_x passivation without Al printing gave a high effective lifetime of 400 μs after firing. All three samples with fritless Al pastes also maintained the effective lifetime around 400-500 μs after the 750°C/3s firing. This demonstrates that firing of a fritless Al paste, with or without the Si content, does not degrade the SiO_2/SiN_x quality. On the other hand, the fritted Al paste lowered the effective lifetime from ~400 μs to 130 μs. This is attributed to the reaction between the glass frit in the paste and the SiO_2/SiN_x layer, resulting in significant degradation of the passivation quality. Thus, fritless Al is a better choice for dielectric back-passivated solar cells.

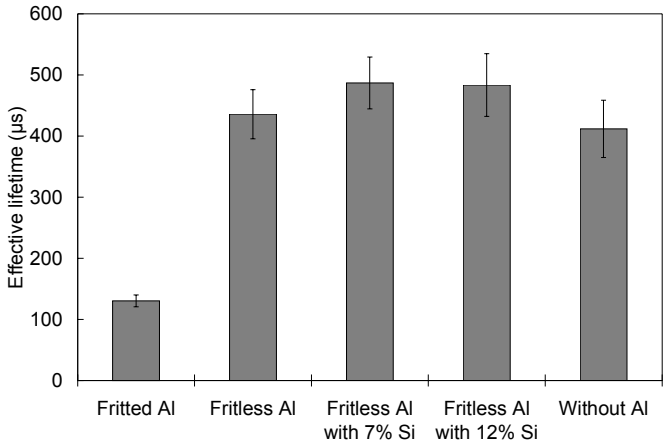


Figure 8.2 Effective lifetimes of SiO_2/SiN_x passivated samples after firing without and with different Al pastes on top.

8.1.2 Effect of the Al paste Composition on the Internal Back Surface Reflectance

Figure 8.3 shows the total reflectance, measured from the front side, in the long wavelength range (900-1,200 nm) for the four different Al pastes printed on 1,000 Å-thick SiN_x on the back and fired at 750°C/3s. Total reflectance of a full-area Al-BSF sample formed with no dielectric and firing of the fritted Al is also shown in Figure 8.3 as a reference. The results show that the four dielectric/metal systems gave significantly higher escape reflectance compared to the full-area Al-BSF structure, indicating superior internal back surface reflectance. However, the presence of Si in the two Al pastes clearly lowered the reflectivity of the metal-dielectric system. Following the method used in [25], the internal back surface reflectance was extracted. The internal back surface reflectance values were found to be 93%, 94%, 89%, 88% for the dielectric/metal system with fritted Al, fritless Al, fritless Al with 7% Si and fritless Al with 12% Si on dielectric, respectively. On the other hand, much lower internal back surface reflectance of 62% was obtained for the conventional full-area Al-BSF structure.

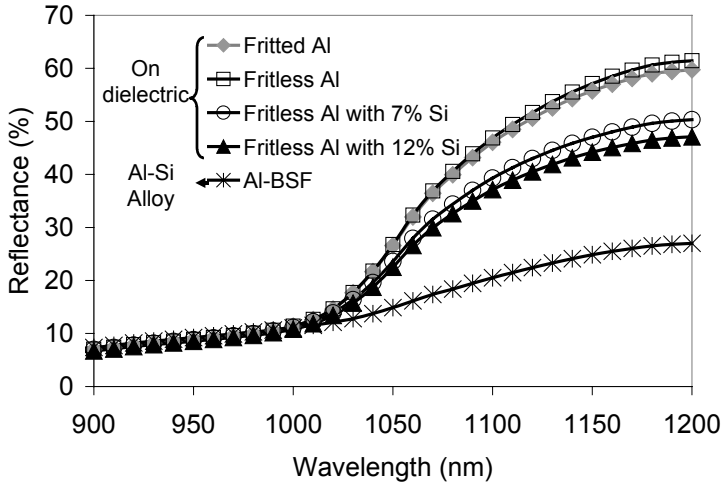


Figure 8.3 Total reflectance in the long wavelength for different back structures.

8.1.3 Effect of the Al Paste Composition on the LBSF Formation

SEM micrographs of the LBSF regions formed by the four Al pastes are shown in Figure 8.4. When the fritted Al or the fritless Al paste without a Si additive is used, the BSF region under the local Al contact is found to be quite thin (< 6 μm). On the other hand, the fritless Al pastes with 7% and 12% Si gave BSF regions that were much thicker (up to 13.5 μm) and more uniform. Based on the observed BSF structure alone, the fritless Al paste with 12% Si should provide the best passivation quality because a thicker p^+ region is more effective in decoupling the back metal.

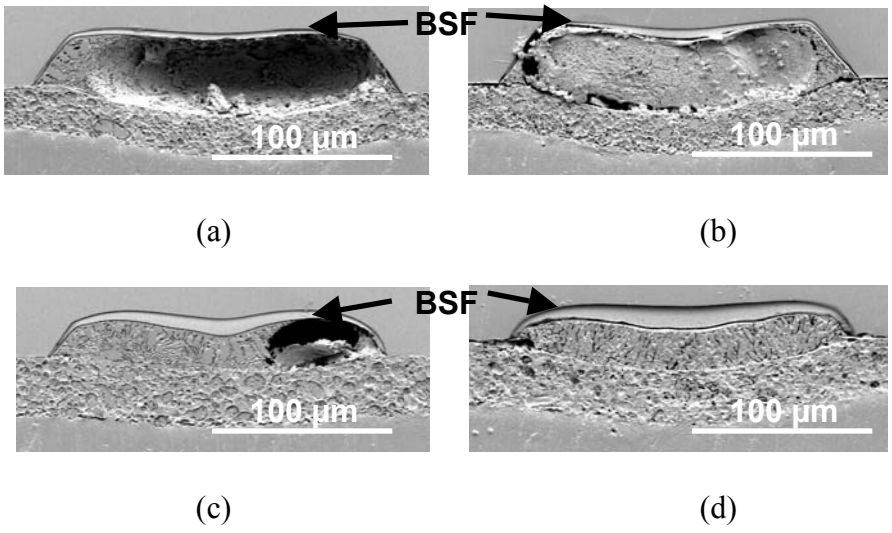


Figure 8.4 Cross-sectional SEM micrographs of the LBSF region for different Al pastes: (a) fritted Al, (b) fritless Al, (c) fritless Al with 7% Si, and (d) fritless Al with 12% Si.

Adding Si to the Al paste increases the depth of the BSF in a local area opening because, in the absence of Si in the Al paste, the Al layer away from the openings needs certain amount of Si to stay in equilibrium during the cool-down from the peak firing temperature. This reduces the amount of Si available for the regrowth in the openings, resulting in a thinner LBSF. Addition of Si to the Al paste satisfies the Si appetite of the surrounding Al and, therefore, most of the Si in the molten Al-Si alloy in the openings is available for the regrowth of Al-doped Si, resulting in a thicker LBSF. The presence of Si in the Al paste is the key to achieving a thicker and superior BSF.

8.1.4 Effect of the Al Paste Composition on the Performance of Dielectric Back-Passivated Solar Cells with a LBSF

After establishing the impact of the Al composition on the passivation quality, the internal reflectance, and the LBSF formation, complete cells were fabricated with the four Al pastes. Efficiency, J_{sc}, V_{oc}, and FF of dielectric back-passivated solar cells with a LBSF fabricated with the four Al pastes are summarized in Figure 8.5a, b, c, and d,

respectively. For comparison, data of a conventional full-area Al-BSF cell with no back dielectric are also included in the figure. Note that the full-area Al-BSF cells were fabricated without the oxidation step; therefore, the front surface passivation is achieved by the SiN_x layer alone, as opposed to an SiO_2/SiN_x layer for the LBSF cells. It can be seen from Figure 8.5 that, for the LBSF structure, the use of the fritless Al pastes with Si additives resulted in a significant improvement in cell performance over the fritted or the fritless Al pastes with no Si. Unfortunately, the LBSF cell efficiency, even with the modified Al-Si pastes, was still lower than that of the conventional full-area Al-BSF cells. This is a result of lower J_{sc} and FF in these LBSF cells. Note, however, that the V_{oc} was higher for the LBSF cells with the Al pastes with Si additives. Reduced J_{sc} and FF, while maintaining high V_{oc}, is most likely a result of the parasitic shunting between the back contact and the SiO_2/SiN_x-induced inversion layer in these LBSF cells.

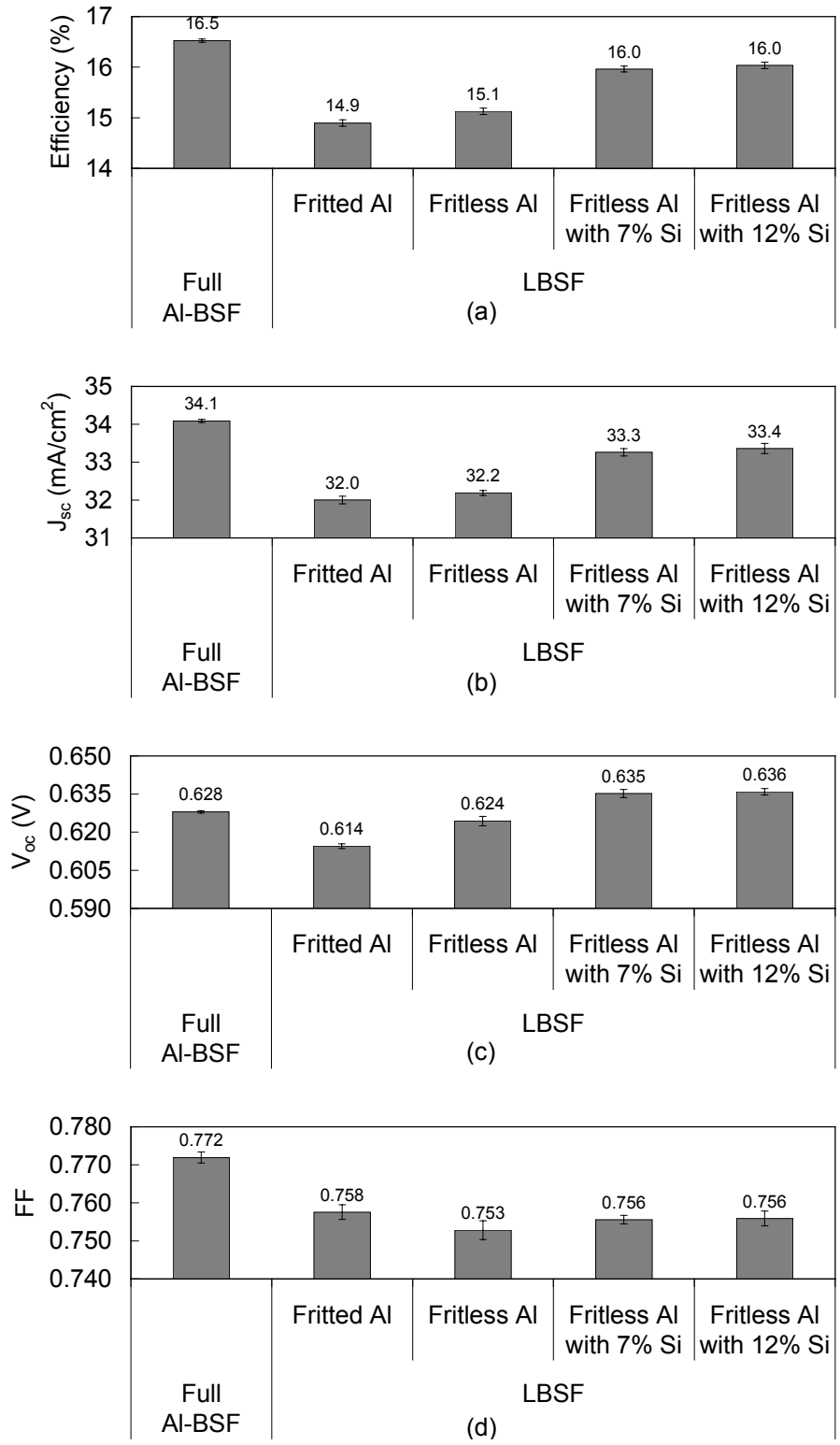


Figure 8.5 Light I-V characteristic of screen-printed solar cells with different structures: (a) Efficiency, (b) J_{sc}, (c) V_{oc}, and (d) FF.

The spatial uniformity of the back surface passivation of the five cells in Figure 8.5 was evaluated using LBIC measurements. The long-wavelength (980 nm) LBIC responses, which are very sensitive to the BSRV, of the five cells (including the full-area Al-BSF cell) are shown in Figure 8.6. The LBIC response at 980 nm was found to be proportional to the J_{sc} values in Figure 8.5b, which suggests that the trend in J_{sc} is dictated by the difference in the BSRV (as the bulk lifetime was quite high (>400 μs) in these FZ samples). The LBSF cell with the fritted Al gave a uniformly poor LBIC response, which is attributed to the degradation of the SiO_2/SiN_x passivation quality because of the etching or interaction between the frit and the SiO_2/SiN_x as well as the poor LBSF. The cell with the fritless Al with no Si gave a better response in between the point contacts (Figure 8.6b) compared to the cell with the fritted Al. However, the response at the point contact was clearly lower than the regions in between because of the poor LBSF. On the other hand, the LBSF cells with Si-added Al pastes showed a better and more uniform LBIC response even at the point contacts. Unfortunately, the overall LBIC response of the LBSF cells with the Si-added pastes were lower than that of the conventional full-area Al-BSF cell. This is attributed to the parasitic shunting of the inversion layer induced by a high positive charge density in the stacked SiO_2/SiN_x layer used in these LBSF cells. Therefore, to take the full advantage of dielectric back passivation, a new dielectric layer that prevents the formation of an inversion layer and can withstand contact firing needs to be developed, which is discussed in detail in the next section.

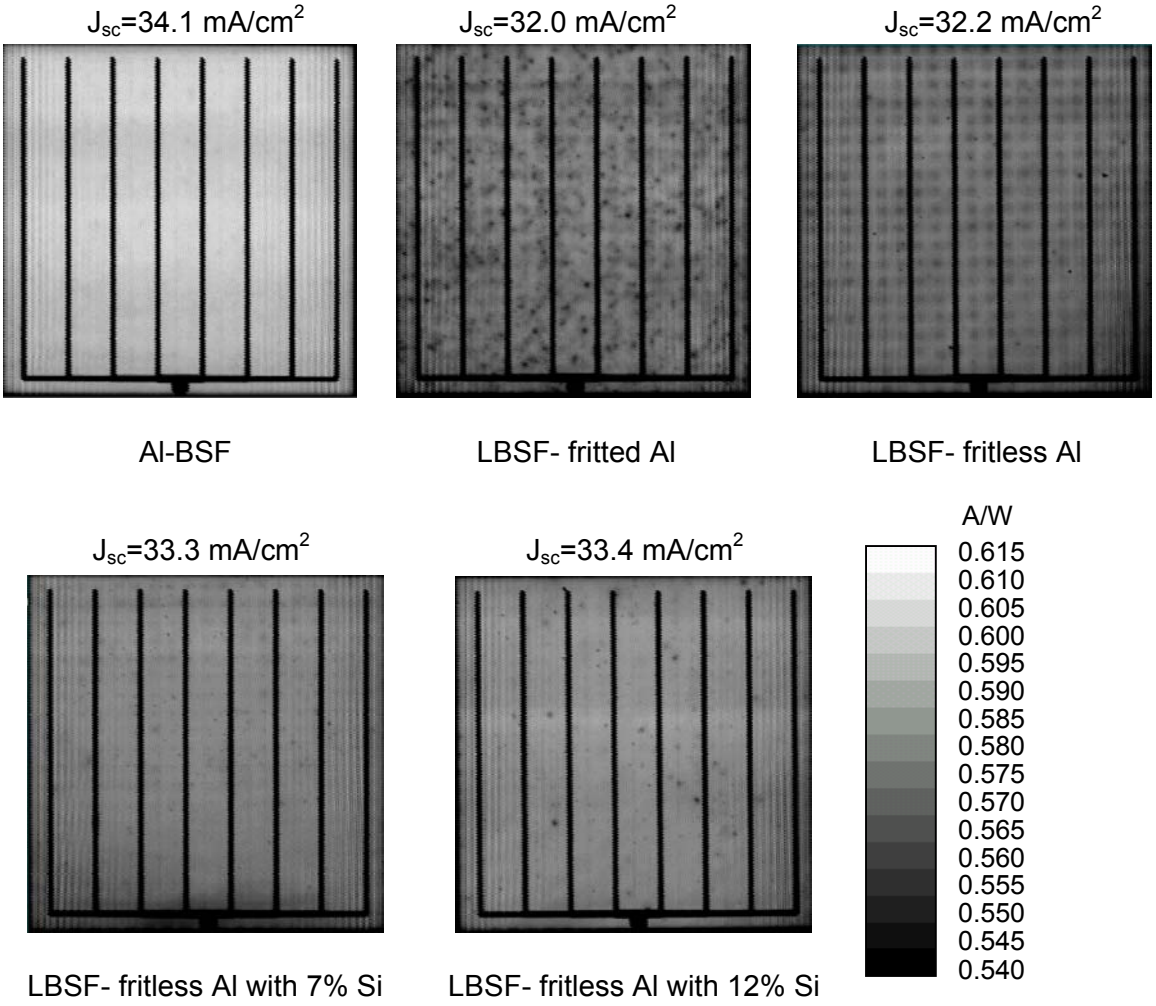


Figure 8.6 Long-wavelength LBIC responses of screen-printed solar cells with different back structures. J_{sc} for each structure from Figure 8.5b is included for comparison.

8.2 Development of Dielectric Layers with Desirable Properties for Back Surface Passivation of p-Type Si Solar Cells

As pointed out at the end of Chapter 7, a suitable dielectric layer for back surface passivation of p-type Si solar cells should contain only either a moderate amount of a positive charge density or a substantial amount of a negative charge density. This is in addition to providing good surface passivation. This is because good passivation is necessary but not sufficient for good cells. A dielectric layer with great passivation will

fail to produce a good cell if it contains high positive charge, which can induce an inversion layer and shunt the device.

In the first part of the study, two new SiO_2-based spin-on dielectric layers along with several conventional dielectric layers were investigated. These dielectric layers were analyzed in terms of their charge and passivation quality. The two new spin-on dielectric layers included in this study were formed using (1) pure SiO_2 silicate as a precursor and (2) SiO_2 silicate and $Al(NO_3)_3$ as a precursor. Conventional dielectric layers included in this study were thermally grown SiO_2, LF-SiN_x (index ~ 2.0), and stacked thermal-SiO_2/LF-SiN_x. Subsequently, in the second part of the study, a similar investigation was conducted on the two new spin-on dielectric layers capped with the LF-SiN_x.

The process to form the spin-on dielectric layers in this study involved: (1) spinning of a sol-gel precursor on a Si substrate, (2) drying at 200°C for 15 minutes, and (3) curing in O_2 ambient for 10 minutes followed by an in-situ 10 minutes anneal in N_2 ambient at 875°C in a conventional tube furnace. Thermally grown SiO_2 in this work (including the one used for the SiO_2/LF-SiN_x stacked layer) was formed using the exact same annealing recipe (10 minutes in O_2 ambient and 10 minutes in N_2 ambient at 875°C), which resulted in an SiO_2 thickness of 80-100 Å on 1-2 ohm-cm p-type Si substrates.

The use of the pure SiO_2 silicate precursor resulted in an SiO_2 layer with a thickness of 2,600 Å. On the other hand, the use of the SiO_2 silicate+$Al(NO_3)_3$ precursor resulted in an Al-doped SiO_2 layer with a thickness of 1,300 Å. It was found that there was no Al-diffusion into the Si substrate during the formation of the Al-doped SiO_2 layer as observed by no change in the sheet resistance of the lightly-doped Si test wafer.

The dielectric charge density and its polarity were measured using a SemiTest SCA-2500 surface charge analyzer. This tool allows a contactless non-destructive measurement of a flat-band equivalent charge density (Q_{FB}, a total charge density at the flat-band condition) in a dielectric layer of interest. The test samples for the charge density measurement were prepared by forming different dielectric layers on 1.2-1.3 ohm-cm p-type FZ Si samples.

The surface passivation quality was assessed by effective lifetime measurements using the photoconductance method. Lifetime test samples were prepared by forming the same dielectric layer on both sides of 2.5 ohm-cm p-type FZ Si samples. All the lifetime values reported in this section were measured at an injection level of 5×10^{14} cm^{-3}.

8.2.1 Investigation of New Spin-On Dielectric Layers and Several Conventional Dielectric Layers for Back Surface Passivation of p-Type Si Solar Cells

Five different dielectric layers, including spin-on SiO_2, spin-on Al-doped SiO_2, thermal SiO_2, stacked thermal SiO_2/LF-SiN_x, and LF-SiN_x were investigated in terms of their charge and their passivation quality. Both charge and effective lifetime measurements were performed at different stages of the following process sequence: (1) as-formed, (2) after an FGA at ~400°C for 30 minutes, (3) after rapid firing in a belt line furnace (with a peak temperature of 700-800°C and a dwelling time of ~ 3s), and (4) after another FGA for 30 minutes. In addition, the long-term stability of these dielectric layers was investigated by leaving the samples for more than six months in open ambient at a room temperature and then re-measuring charge and effective lifetimes.

8.2.1.1 Determination of Charge in the Dielectric Layers

Figure 8.7 shows the measured flat-band equivalent charge densities of the five dielectric layers after different annealing treatments as well as after the six-month period. The charge density in these dielectrics showed a similar pattern as a function of annealing: the amount of charge decreased after an FGA, increased after firing, then decreased again after the second FGA. This is consistent with the fact that, in general, the source of charge in a semiconductor/dielectric system is from unsatisfied bonding either in the dielectric layer or at the dielectric/semiconductor interface. An FGA leads to hydrogenation of the unsatisfied bonds and; hence, decreases the charge density. Rapid firing, on the other hand, tends to disrupt the bonding and; hence, increases the amount of charge.

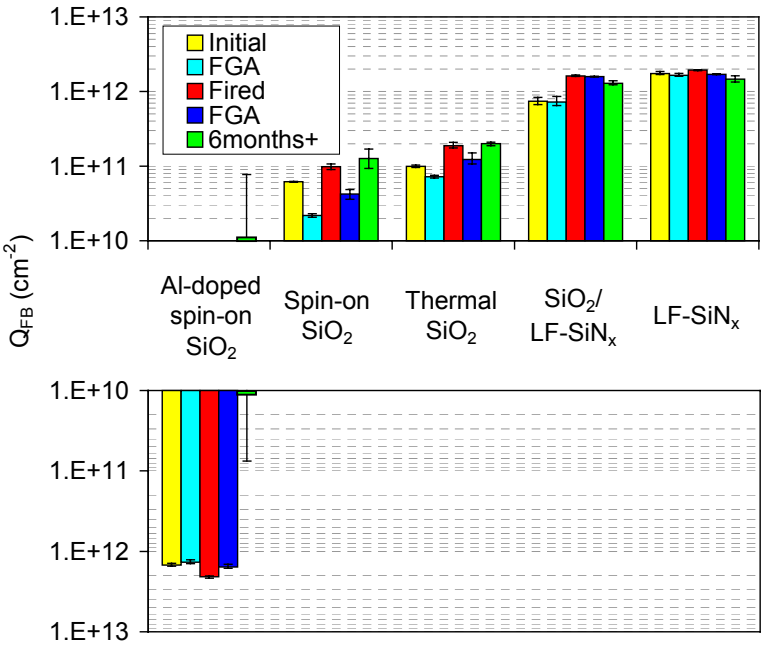


Figure 8.7 Flat-band equivalent charge densities for different dielectric layers.

Figure 8.7 shows that the spin-on SiO_2 and the thin thermally grown SiO_2 exhibited a modest positive charge density of $\leq 2\times10^{11}$ cm^{-2} throughout the process sequence. The charge density stayed at this level after the six-month period. On the other hand, the LF-SiN_x exhibited a much higher positive charge density of $\sim2\times10^{12}$ cm^{-2} throughout the four-step process sequence. The charge density decreased slightly after the six-month period but was still higher than 1×10^{12} cm^{-2}. The charge density of the stacked SiO_2/LF-SiN_x started lower at 8×10^{11} cm^{-2} and decreased slightly to 7×10^{11} cm^{-2} after the first FGA. However, the charge density increased to $\sim2\times10^{12}$ cm^{-2} (the same level as the LF-SiN_x alone) after the firing treatment, and stayed the same after the second FGA. The charge density in this SiO_2/SiN_x stacked layer reduced slightly after the six-month period but remained higher than 1×10^{12} cm^{-2}, similar to the case of the LF-SiN_x. In contrast to the other dielectric layers, the Al-doped spin-on SiO_2 exhibited a high negative charge density of -1 to -2×10^{12} cm^{-2} throughout the annealing sequence. Unfortunately, after the six-month period, the negative charge density in the spin-on Al-doped SiO_2 dropped to a low value in between -7.54×10^{10} to $+7.72\times10^{10}$ cm^{-2}. The instability of the charge in the spin-on Al-doped SiO_2 is attributed to the moisture absorption, which is one of the most common issues in spin-on dielectric.

8.2.1.2 Surface Passivation Quality

Effective lifetimes measured on test samples passivated with the five dielectric layers are summarized in Figure 8.8.

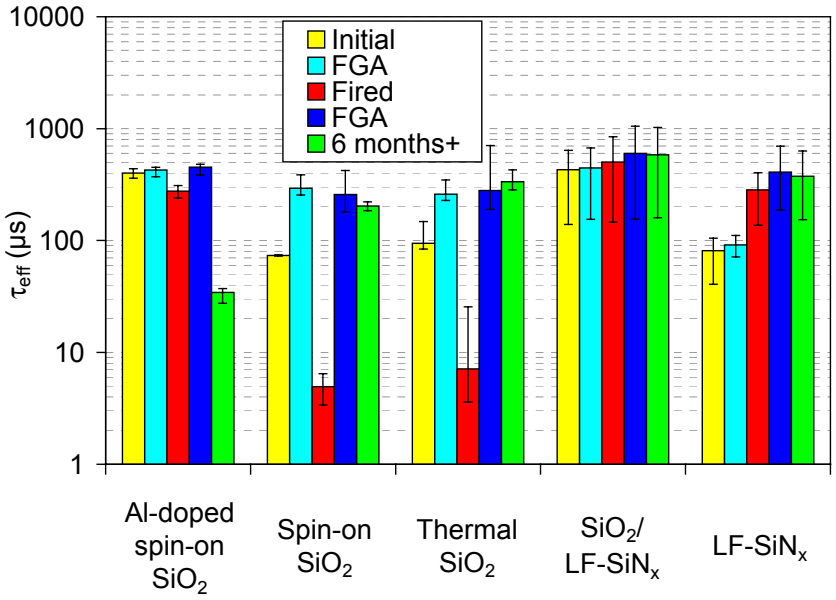


Figure 8.8 Effective lifetimes measured at an injection level of 5×10^{14} cm^{-3} on 2.4-2.5 ohm-cm p-type FZ Si samples passivated with different dielectric layers.

The spin-on SiO_2 and the thin thermally grown SiO_2 again showed a similar behavior, where their effective lifetimes improved significantly from 70-100 µs to 200-300 µs after the first FGA, degraded significantly to 5-10 µs after a firing cycle, and recovered back to 200-300 µs after the second FGA. The passivation quality also stayed the same (with an effective lifetime of 200-300 µs) after the six-month period. These results suggest that the spin-on SiO_2 and the thin thermal SiO_2 require a hydrogenation process to achieve high-quality surface passivation, and their surface passivation quality is not stable against subsequent rapid firing, which could prevent their direct application to screen-printed solar cells.

The surface passivation quality of the SiO_2/LF-SiN_x stack and the LF-SiN_x improved gradually through the four-step annealing sequence. The SiO_2/LF-SiN_x started with a high effective lifetime of ~400 µs and ended up with an effective lifetime of ~600 µs after the final FGA. The LF-SiN_x, on the other hand, started with a lower effective

lifetime of ~70 µs, improved only slightly to ~90 µs after the first FGA, but improved significantly after the firing cycle to ~300 µs, and reached 400 µs after the final FGA. Both the layers also maintained their passivation quality after the six-month period. These results indicate that the LF-SiN_x layer (individually or as a capping layer) provides an excellent protection against the rapid firing cycle, and at the same time serves as an excellent source for hydrogenation of the interface states.

The Al-doped spin-on SiO_2 started with a high effective lifetime of 400 µs that remained unchanged after the first FGA. The effective lifetime decreased slightly to ~250-300 µs after the firing cycle, and recovered back to ~400 µs after the second FGA. Unfortunately, the effective lifetime degraded dramatically to ~35 µs after the six-month period. This is attributed to the loss of the negative charge density in this layer as shown in Figure 8.7. These results revealed that the spin-on Al-doped SiO_2 layer suffered from long-term instability, which makes it unsuitable for the target application.

In conclusion, this study revealed that the LF-SiN_x and the SiO_2/LF-SiN_x layers provide great and stable passivation even after a firing step. Unfortunately, both of them contain an unacceptably high positive charge density. On the other hand, the spin-on SiO_2 and the thin thermal SiO_2 had low and acceptable positive charge, but they completely lost their passivation quality after the rapid firing cycle because of interface quality degradation. The Al-doped SiO_2 layer exhibited the desirable negative charge density and high-quality surface passivation but it suffered from long-term instability where it lost the negative charge density and, hence, the passivation quality after few months. Since all the above dielectric layers failed, the search for the right dielectric was continued by

combining the attributes of the LF-SiN_x and the spin-on dielectric layers in the next section.

8.2.2 Investigation of New Spin-On Dielectric Layers Capped with LF-SiN_x for Back Surface Passivation of P-Type Si Solar Cells

Each of the five dielectric layers in the previous study failed to serve as a back passivation layer of p-type Si solar cells. Based on the findings in the previous section, it was decided to combine the strengths of the LF-SiN_x and the two new spin-on dielectric layers by capping the latter with the LF-SiN_x. Again, charge densities and effective lifetime measurements were used as indicators to assess the suitability of these dielectric systems for the target application.

8.2.2.1 Determination of Charge in the Spin-On Dielectric/LF-SiN_x Stack

Figure 8.9 shows measured flat-band equivalent charge densities as a function of processing steps for the two spin-on dielectric layers capped with the LF-SiN_x. The measurements were performed after (1) curing of the spin-on dielectric, (2) SiN_x deposition on top of the spin-on dielectric, (3) first FGA, (4) rapid firing cycle, (5) second FGA, and (6) after three months aging. FGA and firing cycles were identical to the ones used in the previous section.

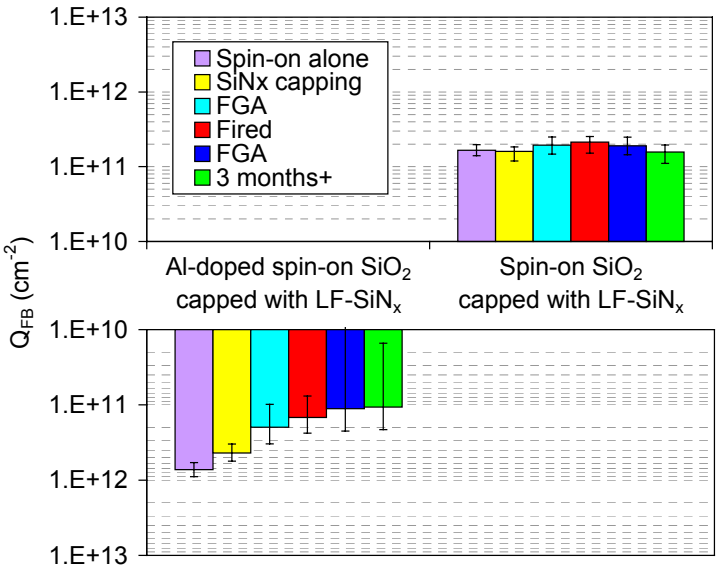


Figure 8.9 Flat-band equivalent charge densities for the two spin-on dielectric layers capped with the LF-SiN_x.

Prior to capping with the LF-SiN_x, the spin-on SiO_2 layer gave a moderate positive charge density of less than 2×10^{11} cm^{-2}. Unlike the thin thermal-SiO_2 investigated in the previous section, the positive charge density remained unchanged after the SiN_x-deposition for the spin-on SiO_2. The charge density also remained the same (at around 2×10^{11} cm^{-2}) for the rest of the heat treatments as well as after the three-month period. On the other hand, the negative charge density in the spin-on Al-doped SiO_2 layer continually decreased, as it went through the annealing. Before it was capped with the LF-SiN_x, it gave a negative charge density of -7×10^{11} cm^{-2} (Note that this value is somewhat lower than the value shown in Section 8.2.1.1 because of the process-induced variation; however, the passivation by the layer (prior to the SiN_x deposition) is still quite effective as will be shown in the subsequent section). The negative charge density decreased to -4.5×10^{11} cm^{-2} after the SiN_x-deposition step. The negative charge density

kept decreasing for the subsequent annealing until it reached ~ -1×10^{11} cm^{-2} after the final FGA. The charge also stayed at this level after the three-month period.

These results suggested that the spin-on SiO_2/LF-SiN_x stack has great potential to be an effective back surface passivation layer for p-type Si solar cells because it exhibits a desirable amount of a positive charge density. On the other hand, the stacked spin-on Al-doped SiO_2/LF-SiN_x might not be suitable for the target application because its negative charge density decreases with annealing.

8.2.2.2 Surface Passivation Quality of the Spin-On Dielectric/LF-SiN_x Stack

Measured effective lifetimes as a function of various processing steps for the two spin-on dielectric layers capped with the LF-SiN_x are shown in Figure 8.10. Before it was capped with the LF-SiN_x, the spin-on SiO_2 gave a low effective lifetime of ~60 μs. After the SiN_x deposition, the effective lifetime improved dramatically to ~700 μs. This effective lifetime value remained virtually the same after the first FGA and subsequent rapid firing. The final FGA improved the effective lifetime even further to ~1.5 ms. Finally, after the three-month period, the effective lifetime reduced slightly to ~1.3 ms.

On the other hand, the spin-on Al-doped SiO_2 by itself, with no SiN_x capping, gave a high effective lifetime of ~450 μs, which decreased drastically to ~40 μs after the SiN_x deposition. The effective lifetime stayed between 30 and 50 μs after the remaining processing steps as well as after the three-month aging period. The drop in the effective lifetime after the SiN_x deposition is attributed to the loss of the negative charge density in this layer shown in the previous section.

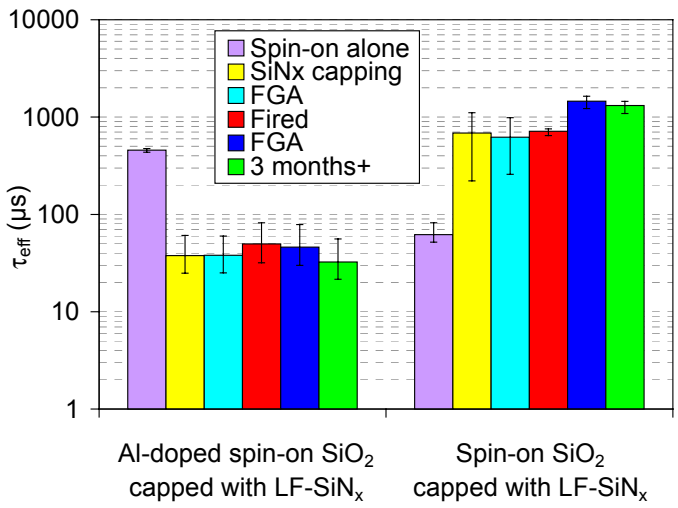


Figure 8.10 Effective lifetimes measured at an injection level of 5×10^{14} cm^{-3} on 2.4-2.5 ohm-cm p-type FZ Si samples passivated with the spin-on dielectric layers capped with the LF-SiN_x.

In conclusion, the spin-on SiO_2/SiN_x stack shows great potential to be an effective back surface passivation layer for p-type Si solar cells. It provides an excellent passivation quality even after firing, and also exhibits a positive charge density in the suitable range. In contrast, the stacked spin-on Al-doped SiO_2/SiN_x shows a poor passivation quality immediately after the SiN_x deposition step. This is attributed to the decrease in the negative charge density by the presence of the SiN_x layer, which could be caused by charge neutralization by hydrogenation or charge cancellation by the positive charge density in the LF-SiN_x film.

8.3 Conclusions

This chapter covered two novel areas of development for achieving low-cost dielectric back-passivated p-type Si solar cells. The first area involves development of a low-cost screen-printing process to simultaneously form a high-quality self-aligned LBSF in conjunction with the formation of a back surface reflector for dielectric back-

passivated p-type Si solar cells. A new Al paste was developed and used to successfully form a uniform and thick (>10 μm) LBSF layer through the openings in the dielectric without deteriorating the passivation quality of the dielectric elsewhere. The modification to the Al paste involved removal of glass-frit and an addition of Si (7-12%) to the paste. The modified Al paste resulted in a significant improvement (of ~1% absolute higher efficiency) in LBSF cell performance compared to when a conventional Al paste was used. However, the efficiency of the LBSF cells, even with the modified Al pastes, was lower than that of a conventional full-area Al-BSF cell because of the inferior J_{sc} and FF. This is attributed to the parasitic shunting between the back contact and the inversion layer, which is formed because of the high positive charge density ($>1\times10^{12}$ cm^{-2} after firing) in the SiO_2/SiN_x layer used in this study. This led to the second area of development in this chapter, which involved a dielectric layer that can provide not only high-quality surface passivation but also contain a small positive charge density ($<3\times10^{11}$ cm^{-2}) or a high negative charge density.

In the second area of investigation, two new spin-on dielectric layers were developed and studied in conjunction with several commonly used dielectric layers. Spin-on dielectrics were spun-on, dried and then annealed at 875°C for 10 minutes in O_2 and 10 minutes in N_2. The new spin-on Al-doped SiO_2, one of the two spin-on dielectric layers investigated, was found to exhibit a high negative charge density ($\geq7\times10^{11}$ cm^{-2}) and an excellent surface passivation quality ($S \leq 40$ cm/s on 2.5 ohm-cm Si) immediately after it was formed. However, the layer suffered from long-term instability that caused the negative charge density to decrease, which in turn resulted in a loss of the passivation quality over time. The second spin-on dielectric layer, pure spin-on SiO_2, was found to

behave similarly to the thin thermal-SiO_2 (formed at 875°C for 10 minutes in O_2 and 10 minutes in N_2). Both of them contained a low positive charge density ($\leq 2\times10^{11}$ cm^{-2}) and required a hydrogenation step to achieve high-quality surface passivation ($S \leq 60$ cm/s on 2.5 ohm-cm Si). Unfortunately, their passivation quality degraded (S~3,500 cm/s) upon a rapid contact firing cycle (700-800°C/3s), which would prevent their direct application to screen-printed solar cells. The LF-SiN_x and the stacked thin thermal-SiO_2/LF-SiN_x films provided high-quality surface passivation and high thermal stability against the contact firing cycle, but because of a high positive charge density ($>1\times10^{12}$ cm^{-2}), they became undesirable for the target application.

Based on the above characterization and understanding, an effort was made to combine the strength of the LF-SiN_x layer for its thermal stability with respect to a firing cycle and the strengths of the two new spin-on dielectric layers for their passivation quality and charge density. This was accomplished by capping the pure spin-on SiO_2 and the Al-doped spin-on SiO_2 with the LF-SiN_x. Capping the spin-on Al-doped SiO_2 with the LF-SiN_x caused significant degradation in the passivation quality, which was attributed to the reduction in the negative charge density because of the presence of the LF-SiN_x film. This may be attributed to charge neutralization by hydrogenation or charge cancellation by the positive charge density in the LF-SiN_x film. On the other hand, the spin-on SiO_2/LF-SiN_x stack resulted in the right dielectric system, which gave an excellent passivation quality (S~20-25 cm/s on 2.5 ohm-cm Si), high thermal stability against subsequent firing, and a positive charge density in a desirable range ($<3\times10^{11}$ cm^{-2}). Thus, of all the dielectric layers investigated in this chapter, the stacked spin-on SiO_2/SiN_x showed the highest potential to be an effective back surface passivation layer

for p-type Si solar cells, and was selected for the final device fabrication in Chapter 9 of this thesis.

CHAPTER 9

FABRICATION AND ANALYSIS OF SCREEN-PRINTED DIELECTRIC BACK-PASSIVATED SOLAR CELLS WITH A LOCAL BACK SURFACE FIELD

Screen-printed dielectric back-passivated p-type Si solar cells were fabricated using the process proposed at the end of Chapter 7. The metallization technique discussed in Section 8.1 and the spin-on SiO_2/LF-SiN_x dielectric stack discussed in Section 8.2 were implemented in the cell fabrication sequence. The completed cells were first characterized by light I-V measurements. The best cell was then chosen for further characterizations and analyses to provide in depth understanding of high efficiency dielectric back-passivated cells achieved in this research. For comparison, a conventional full-area Al-BSF cell that has a similar front structure is used as a reference. The chapter is divided into three main sections: (1) detail of the fabrication process, (2) characterization of the cells, and (3) simulation of the light I-V characteristics of the cells.

9.1 Development of a Process Sequence to Fabricate Screen-Printed Dielectric Back-Passivated Solar Cells

To demonstrate the efficacy of the new Al-Si paste and the spin-on SiO_2/LF-SiN_x dielectric, following process sequence was used to fabricate the screen-printed dielectric back-passivated p-type Si solar cell in this chapter (Figure 9.1).

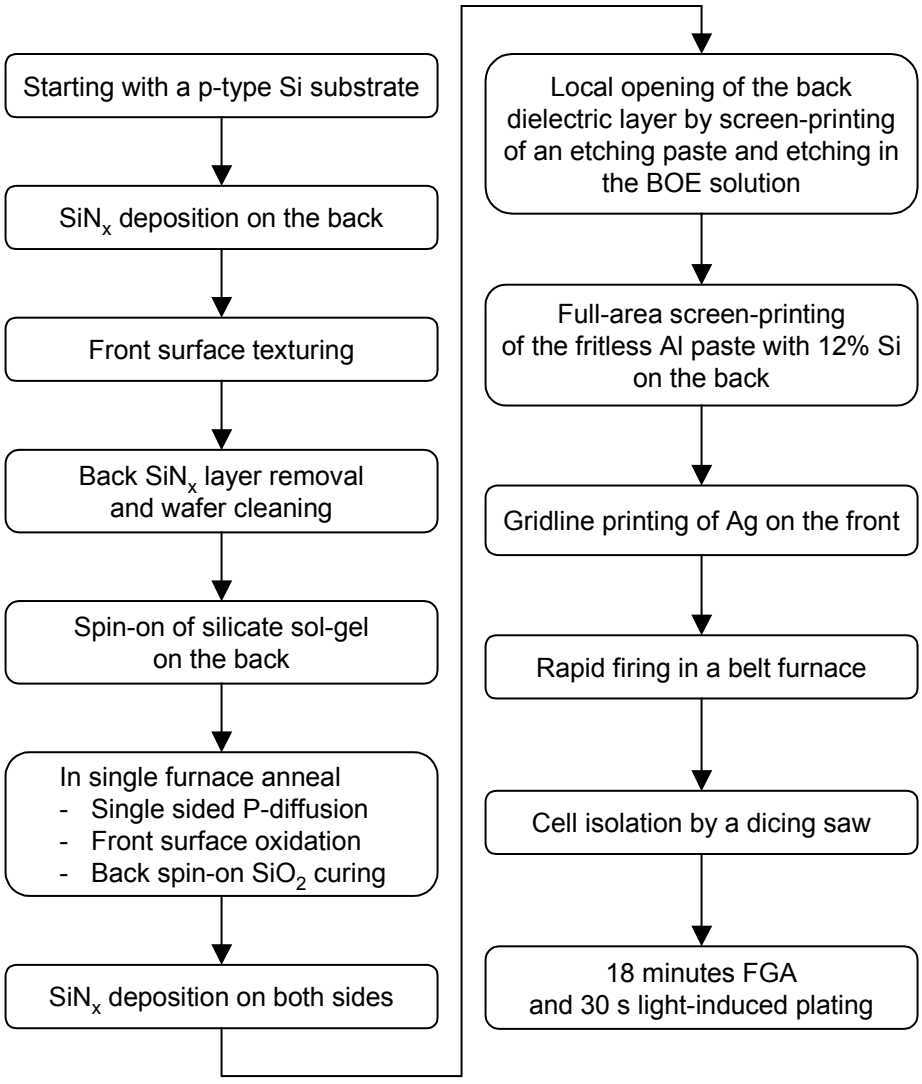


Figure 9.1 Process sequence to fabricate screen-printed dielectric back-passivated p-type Si solar cells in this work.

LF-SiN_x was first deposited on the backside of a 1.3 ohm-cm B-doped FZ Si sample followed by alkaline surface texturing. The LF-SiN_x layer protected the back surface of the sample so that only the front surface was chemically textured, while the back surface remained planar. The LF-SiN_x layer was then removed in a dilute HF solution. Subsequently, the sample was subjected to standard RCA cleaning. After the cleaning, the silicate precursor was spun on the back surface and dried at 200°C for 15 minutes

followed by a P-diffusion process at 875°C (by the limited source technique discussed in [129]) to obtain an n-type emitter with a sheet resistance of ~70-85 ohm/sq. The diffusion took place only on the front surface as the spin-on dielectric layer acted as a diffusion mask to prevent P-diffusion on the back surface.

During the same high temperature cycle, immediately after the P drive-in step, the sample was oxidized for 10 minutes in O_2 ambient followed by 10 minutes curing in N_2 ambient. This provided curing of the spin-on SiO_2 on the rear in conjunction with a thin thermally grown SiO_2 layer on the front surface for enhanced surface passivation. Subsequently, LF-SiN_x was deposited on both sides of the sample, resulting in a stacked thermal-SiO_2/LF-SiN_x layer on the front surface and a stacked spin-on SiO_2/LF-SiN_x layer on the back surface. Local openings of the back dielectric were then formed by (1) screen-printing of SolarEtch paste with a screen design of 100 μm × 100 μm square openings and a center-to-center spacing of 800 μm, (2) annealing at 350°C for 30 s to activate the etching reaction, (3) rinsing to remove the etching residue, and (4) etching in buffered oxide etchant (BOE) for one to three minutes to completely remove the spin-on SiO_2 layer in the openings while using the SiN_x as a mask.

After the back dielectric opening step, the fritless Al paste with 12% Si was screen-printed on the entire back surface, followed by screen-printing of Ag gridlines on the front surface. The sample was then fired in a belt furnace at a peak temperature of ~800°C for ~3 s. Nine 2×2 cm^2 cells were isolated by a dicing saw followed by an 18-minute FGA and a 30-s light-induced plating [130]. The finished cells were fully characterized to understand the performance enhancement because of dielectric back

passivation relative to the full-area Al-BSF, which is the topic of discussion in the next section.

9.2 Characterization and Analysis of the Screen-Printed Dielectric Back-Passivated Solar Cell

The dielectric back-passivated cells were first characterized by light I-V measurements, which provided important cell parameters including J_{sc}, V_{oc}, FF, efficiency, n-factor, series resistance (R_s) and shunt resistance (R_{sh}) (the methods used to extract n-factor, R_s, and R_{sh} are explained in detail in [131]). More detail characterization was performed on the best dielectric back-passivated cell including (1) dark I-V measurements to obtain the junction leakage property, (2) long-wavelength LBIC mapping to study the spatial uniformity of the back passivation, (3) spectral response and total reflectance measurements to obtain the IQE and the reflectance properties, and (4) photoconductance decay lifetime measurement to obtain the bulk recombination lifetime. Finally, the effective front surface recombination velocity (FSRV) and the effective BSRV were extracted by fitting the measured IQE in the PC1D simulation program. A conventional full-area Al-BSF cell with a similar front structure (high sheet resistance emitter with stacked thermal SiO_2/SiN_x passivation) was used as a reference to quantify the improvement because of the dielectric back passivation.

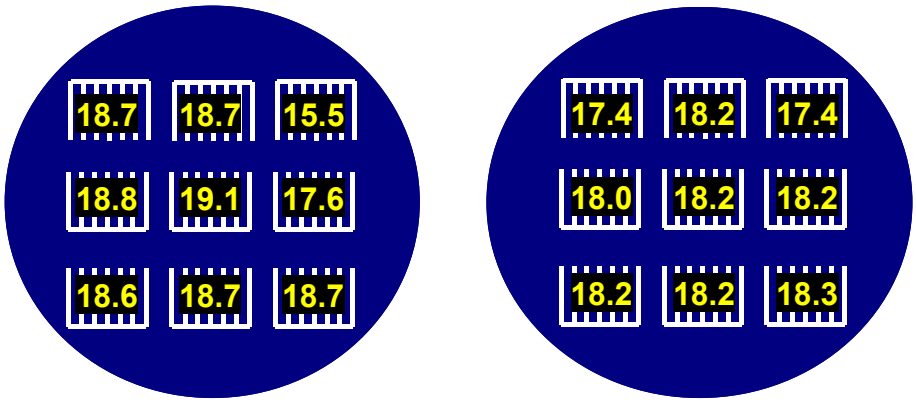
9.2.1 Light I-V Measurement

Following the characterization methods described in [131], V_{oc}, J_{sc}, FF, efficiency, n-factor, R_s, and R_{sh} were extracted for the dielectric back-passivated cells and the full-area Al-BSF reference cells. These parameters are summarized in Table 9-1. In addition, the

efficiency distribution of the nine cells on one large wafer for the two kinds of cells is shown in Figure 9.2.

Table 9-1 Illuminated solar cell characteristic of the dielectric and full-area Al-BSF back-passivated cells.

Name	V_{oc} (V)	J_{sc} (mA/cm^2)	Eff (%)	FF(%)	n-factor	R_s (ohm-cm^2)	R_{shunt} (ohm-cm^2)
Dielectric back-passivated cells							
D1	0.653	38.85	18.61	73.33	1.42	1.03	14540
D2	0.655	38.71	18.72	73.85	1.44	0.91	13860
D3	0.651	38.59	18.74	74.61	1.37	0.87	-220700
D4	0.654	38.91	18.83	74.05	1.39	0.95	-398900
D5	0.654	38.94	19.07	74.83	1.39	0.79	35540
D6	0.644	37.51	17.59	72.79	1.47	1.08	163500
D7	0.653	38.82	18.69	73.72	1.45	0.91	9200
D8	0.654	38.67	18.74	74.10	1.46	0.82	167800
D9	0.643	37.54	15.53	64.30	1.50	3.18	21770
AVG	0.652	38.62	18.28	73.91	1.42	0.92	-26895
Al-BSF cells							
B1	0.641	37.46	18.19	75.83	1.43	0.50	-441900
B2	0.640	37.30	18.22	76.36	1.38	0.48	133300
B3	0.643	37.42	18.28	76.04	1.37	0.57	84000
B4	0.640	37.32	18.00	75.44	1.47	0.51	30850
B5	0.639	37.25	18.17	76.31	1.40	0.45	6464
B6	0.641	37.27	18.23	76.39	1.36	0.52	26550
B7	0.638	37.34	17.37	72.99	1.52	0.90	88740
B8	0.642	37.32	18.20	76.00	1.41	0.52	67670
B9	0.644	37.64	17.42	71.91	1.43	1.25	25580
AVG	0.640	37.33	18.01	75.67	1.42	0.56	-541



(a) Dielectric back (b) Al-BSF back

Figure 9.2 Efficiency distributions of cells fabricated in this study: (a) dielectric back passivation and (b) full-area screen-printed Al-BSF passivation.

In general, the dielectric back-passivated cells gave about 0.3-0.8% higher absolute efficiency than the full-area Al-BSF cells. This is the result of the higher V_{oc} (of >10 mV) and the higher J_{sc} (of 1.3-1.5 mA/cm^2). However, the FF in the dielectric back-passivated cells was somewhat inferior (73.9 as opposed to 75.7) mainly because of the higher R_s. Highest efficiency of 19.1% and 18.3% were obtained for the dielectric and the Al-BSF back-passivated cells, respectively. The efficiency of 19.04% (cell D-5) was also confirmed independently at NREL. The measured light J-V curves of these two screen-printed cells (dielectric back and Al-BSF) are plotted in Figure 9.3. These two cells (D-5 and B-3) were then chosen for detail characterizations, modeling, and analyses in the following sections.

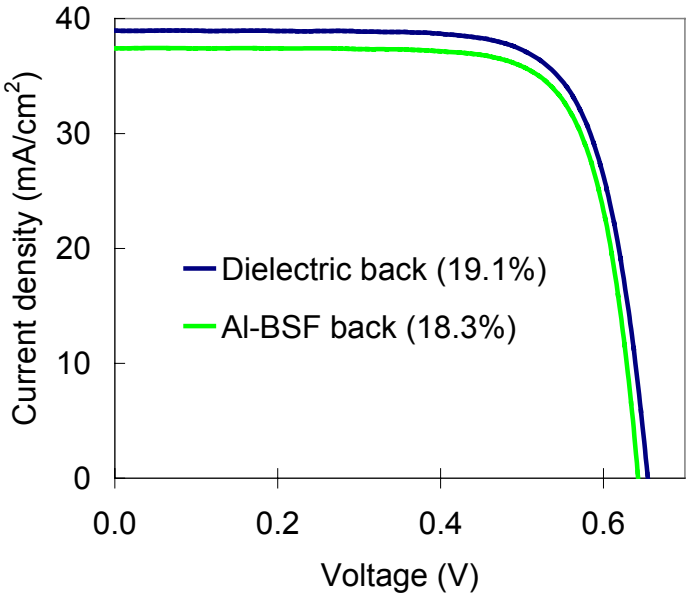


Figure 9.3 Light I-V curves of the best cells in this study: one with dielectric back passivation and the other with full-area Al-BSF passivation.

9.2.2 Dark I-V Measurement

Figure 9.4 shows the dark I-V curves for the dielectric and the Al-BSF back-passivated cells (D-5 and B-3).

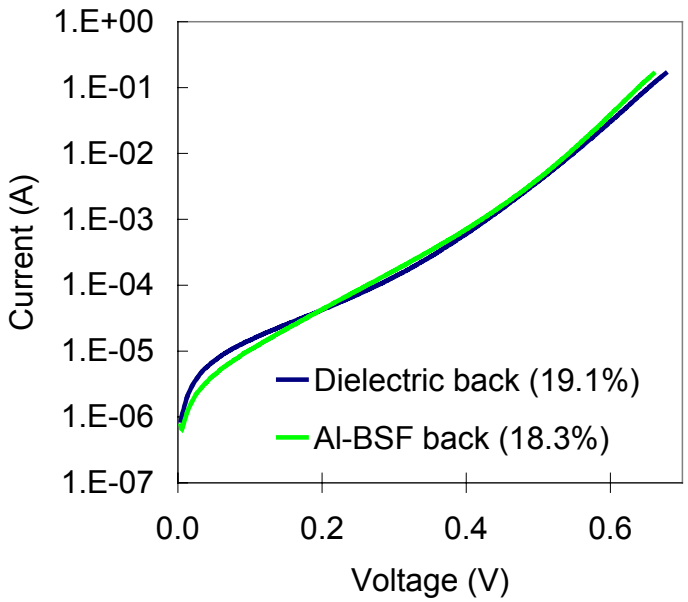


Figure 9.4 Dark I-V characteristics of the dielectric and the Al-BSF back-passivated cells.

Generally, the dark I-V characteristics of a Si solar cell (i.e., a p-n junction semiconductor device) is described by two diodes and two resistance components shown in Figure 9.5. The 1st diode (governing I_{d1}) represents the solar cell itself while the 2nd diode (governing I_{d2}) represents a leakage or recombination in the depletion region of the p-n junction.

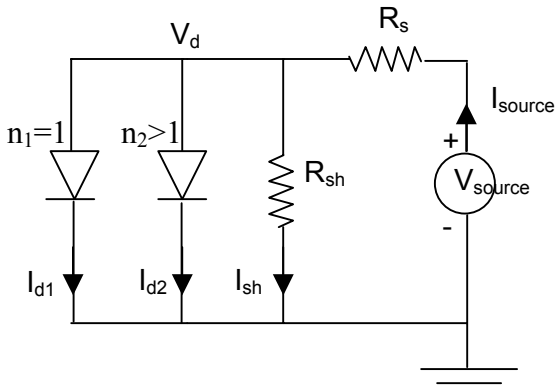


Figure 9.5 Schematic of the double-diode model along with R_{sh} and R_s, representing the Si solar cell operation in the dark.

The two equations describing the source current (I_{source}) and the source voltage (V_{source}) in Figure 9.5 are as follows:

$$I_{source} = I_{d1} + I_{d2} + I_{sh} = I_{01} e^{\frac{qV_d}{kT}} + I_{02} e^{\frac{qV_d}{n_2 kT}} + \frac{V_d}{R_{sh}} \quad \text{and} \tag{9.1}$$

$$V_d = V_{source} - I_{source} R_s \ , \tag{9.2}$$

where I_{01} is the reverse saturation current of the 1st diode, I_{02} is the reverse saturation current of the 2nd diode, and n_2 is the diode ideality factor of the 2nd diode.

A theoretical fit to the dark I-V curve, using five variables in Equations 9.1 and 9.2, should provide information about I_{01}, I_{02}, n_2, R_{sh}, and R_s. To reduce the number of variables from five to three in the fitting routine, R_{sh} was fixed to the value measured by the light I-V measurements in Section 9.2.1, and R_s was calculated using the following equation [132]:

$$R_s = \frac{V_a - V_{oc}}{I_{sc}} \ , \tag{9.3}$$

where V_a is the applied voltage to obtain current equaled to I_{sc} during the dark I-V measurement.

Table 9-2 shows the J_{01}, J_{02}, and n_2 values for the two cells obtained from the dark I-V fitting.

Table 9-2 Extracted R_s, J_{01}, J_{02}, and n_2 of the dielectric and the Al-BSF back-passivated cells from dark I-V analyses.

Parameter	Dielectric back-passivated cell	Al-BSF back-passivated cell
$R_{s,dark}$ (ohm-cm^2)	0.50	0.36
J_{01} (fA/cm^2)	0.24	0.48
J_{02} (nA/cm^2)	142	397
n_2	2.24	2.55

The extracted J_{02} values were quite high for both the cells indicating that there is significant amount of leakage in the junction of both the cells. This suggested the need for development of the front contact formation and the emitter profile. It is noteworthy that the J_{01} value was about a factor of two lower for the dielectric back-passivated cell, which is consistent with the higher V_{oc} in this cell (Table 9-1).

9.2.3 Long-Wavelength LBIC Mapping

To evaluate the uniformity of the back surface passivation, long-wavelength (980 nm) LBIC mapping was performed on the two cells. LBIC maps for the two cells are shown in Figure 9.6. Both the cells exhibited relatively uniform long-wavelength LBIC response. Additionally, the LBIC response of the dielectric back-passivated cell was superior to that of the Al-BSF back-passivated cell, indicating a superior back passivation quality, a superior back internal reflection, or both. A relatively uniform response of the dielectric back-passivated cell also confirmed the effectiveness of the LBSF formed by the Al paste with 12 % Si.

In the next section, reflectance and IQE measurements were performed to further evaluate the optical and the electrical qualities of the two cells.

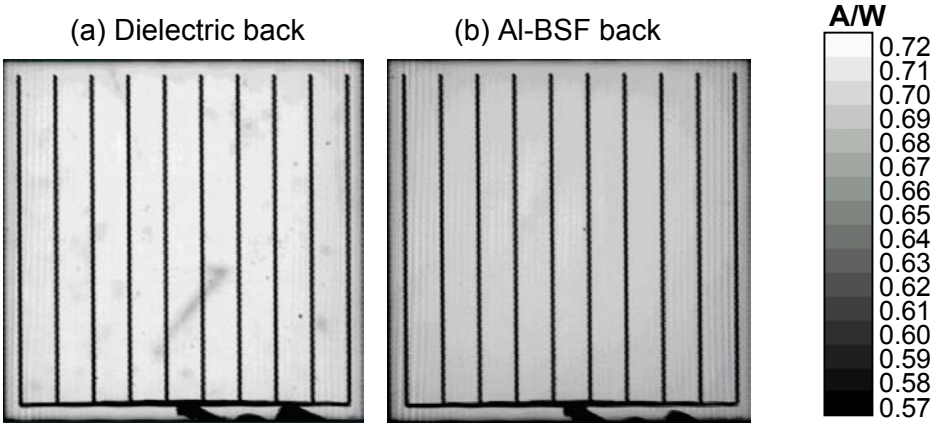


Figure 9.6 Long-wavelength LBIC responses of (a) the dielectric back-passivated cell and (b) the Al-BSF back-passivated cell.

9.2.4 Reflectance and IQE Measurements

The measured total reflectance (350-1,200 nm) of the two cells is shown in Figure 9.7. The reflectance of the two cells was identical for the wavelength below 1,000 nm, indicating that texturing and antireflection coating were very similar. However, the escape reflectance ($\lambda \geq$ 1,000 nm) of the dielectric back-passivated cell was much higher than that of the Al-BSF back-passivated cell. The higher escape reflectance is an indication of better internal back surface reflectance, as described in Section 8.1.

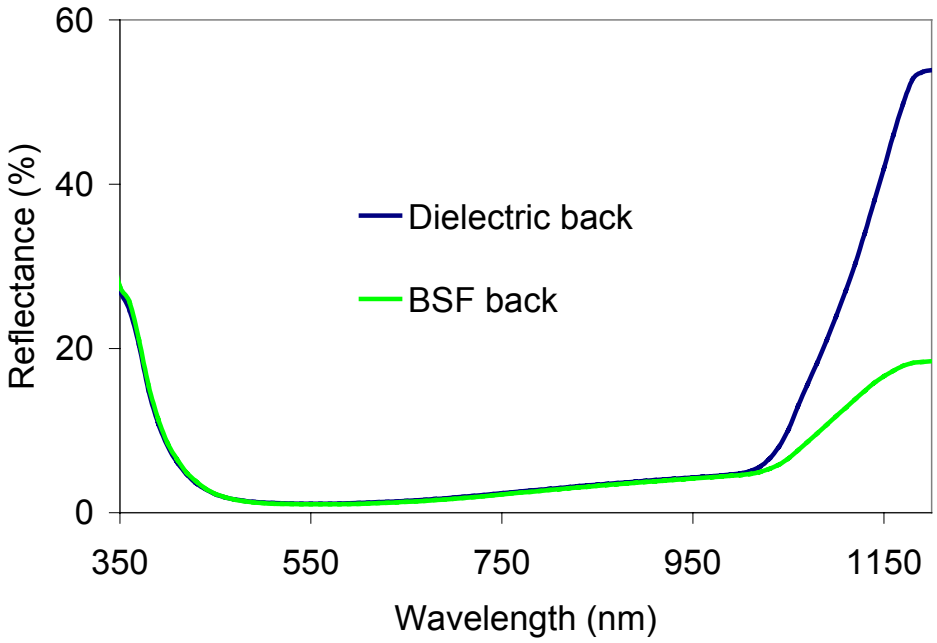


Figure 9.7 Measured total reflectance of the dielectric and the Al-BSF back-passivated cells.

Next, spectral response measurements (350-1,200 nm) were performed on the two cells. Because the LBIC responses were found to be relatively uniform for both the cells, the spectral response measurements were performed only at two locations on each cell, and the average of the two measurements was taken for further analysis. Also note that the spectral response measurements were performed both with and without a constant

one-sun light bias. Subsequently, IQE was calculated from the measured spectral responses and the measured total reflectance. The IQE responses of the two cells with and without light bias are shown in Figure 9.8.

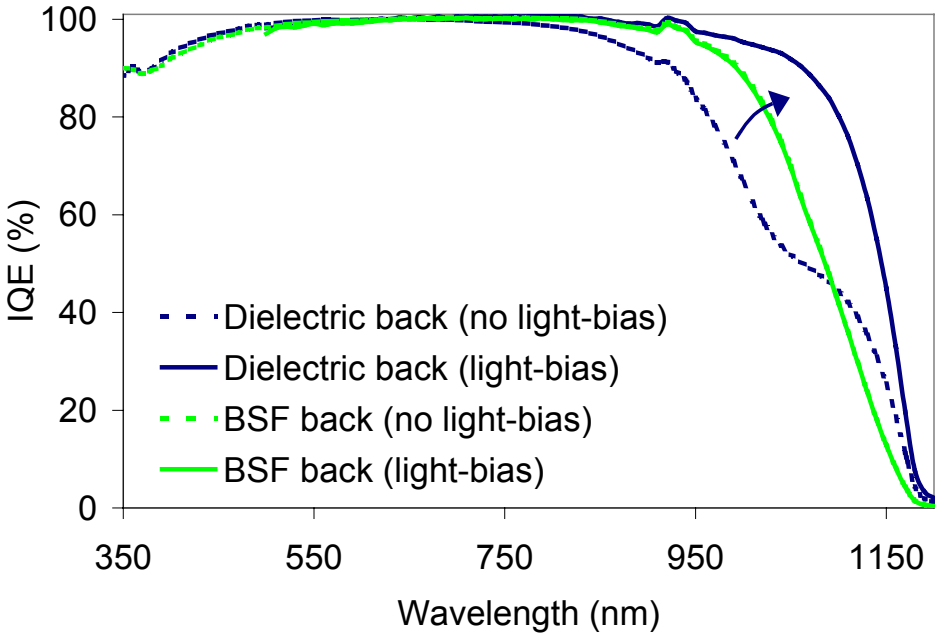


Figure 9.8 Measured IQE responses of the dielectric and the Al-BSF back-passivated cells. The spectral responses were measured with and without one-sun light-bias for both the cells.

The short-wavelength IQE response of the two cells was very similar, confirming the similarity of the emitter and the front surface passivation qualities. In contrast, the long-wavelength response was very different for the two cells. In the case of the dielectric back-passivated cell, the long-wavelength response changed very significantly with and without the light bias. This behavior was absent in the Al-BSF back-passivated cell, where the long wavelength response was virtually the same with and without the light bias. As a result, without the one-sun light bias, the long-wavelength IQE response of the dielectric back-passivated cell was inferior to that of the Al-BSF back-passivated cell, but an opposite trend was observed with one-sun light bias IQE. This peculiar behavior of the

dielectric back-passivated cell can be explained on the basis of strong injection level dependence of the BSRV in the dielectric back-passivated cells. This phenomenon is discussed in detail later in this chapter.

9.2.5 Extraction of Bulk Minority-Carrier Lifetimes in the Finished Cells

The bulk lifetimes in the dielectric and the Al-BSF back-passivated cells were measured with the help of the adjacent cells that went through the same processes. The lifetime was measured by stripping the cells down to the Si substrate and then performing photoconductance decay measurements with surfaces passivated by an iodine/methanol solution. The lifetime at an injection level of 1×10^{14} cm^{-3} for the dielectric and the Al-BSF back-passivated cells was found to be 1,070 μs and 460 μs, respectively. Although, the lifetime in the Al-BSF back-passivated cell was found to be somewhat inferior to that of the dielectric back-passivated cell, the absolute lifetime value of 460 μs is sufficiently high such that it will not account for any performance degradation. This is because the corresponding diffusion length of 1,150 μm for a lifetime of 460 μs in the Al-BSF cell was greater than three times the cell thickness (~300 μm). The high lifetime in the dielectric back-passivated cell is a proof that the process developed in this study does not cause degradation in the bulk lifetime.

9.2.6 Extraction of FSRV and BSRV

From the measured bulk lifetimes and the measured IQE responses, the FSRV and the BSRV were extracted by fitting short- and long-wavelength IQE in the PC1D program, respectively. Prior to the IQE curve fitting, the information of the internal reflection was extracted. This was done by fitting the escape reflectance ($\lambda\geq900$ nm) in the PC1D program. To achieve this, first, the front external reflectance (without escape reflectance)

of each cell was obtained by replacing the measured total reflectance from 900 nm to 1,200 nm with linearly extrapolated values from 900 nm. This was then used as front external reflectance input to the PC1D program. Additionally, the "front surface textured" feature in the PC1D program is activated (more information on this feature can be found in [133]). This feature, when activated, performed two tasks: (1) it incorporates the enhanced recombination at or near the textured front surface because of the larger surface area and (2) it modifies the optical generation to take into account the oblique path traveled by photons through the device. This feature is activated for all the PC1D simulation in this chapter to account for the effect of textured surfaces in the actual cells. The internal reflectance parameters (front and back surface internal reflectance are illustrated in Figure 9.9) were then varied in the PC1D program to match the measured total reflectance in the wavelength range of 900-1,200 nm. The parameters those gave the best fit to the measured total reflectance are summarized in Table 9-3 and the fitted reflectance curves are shown in Figure 9.10.

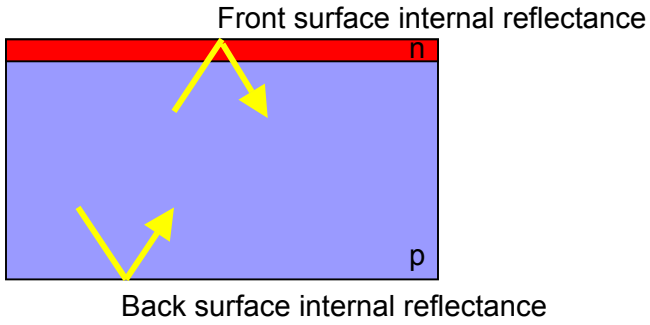


Figure 9.9 Schematic representation of front and back surface internal reflectance.

Table 9-3 Parameters used in the PC1D program to obtain the best fit of the total reflectance in the wavelength range of 900-1,200 nm of the dielectric and the Al-BSF back-passivated cells.

Parameters		Dielectric back	BSF back
Front internal reflection (specular) (%)	1st bounce	84	92
	Subsequent bounce	91	92
Back internal reflection (diffused) (%)	1st bounce	96	68
	Subsequent bounce	93	68
Front surface		Textured: angle 54.74°, depth 3.535 µm	
Substrate thickness		300 µm	

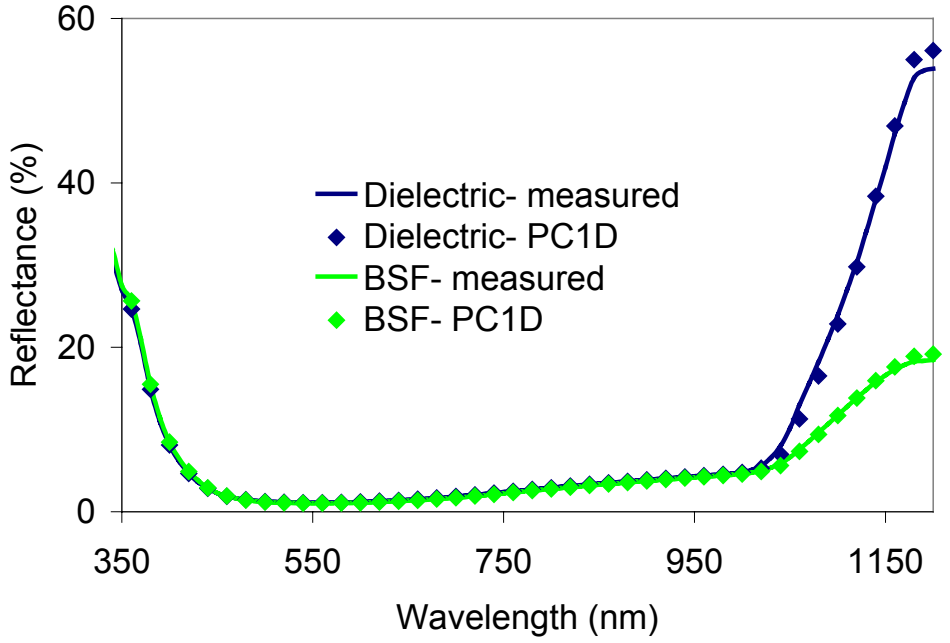


Figure 9.10 Comparison of the measured and the PC1D-simulated reflectance of the dielectric and the Al-BSF back-passivated cells. The parameters used in the simulations are summarized in Table 9-3. Note that the PC1D was used to fit only the wavelength range of 900-1,200 nm (see text for more detail).

The FSRV and the BSRV were then extracted by varying their values to match the measured IQE with the simulated IQE in the PC1D program, using the measured bulk lifetime as one of the inputs. Figure 9.11 shows the emitter profile used in the simulation,

which was obtained from the spreading resistance measurements. The spreading resistance measurements were performed on two locations of a polished Si sample that went through the similar diffusion process for each of the two cells.

The parameters used in the PC1D program that gave the best fit to the IQE curves of the two cells are summarized in Table 9-4 and the fitted IQE curves are shown in Figure 9.12.

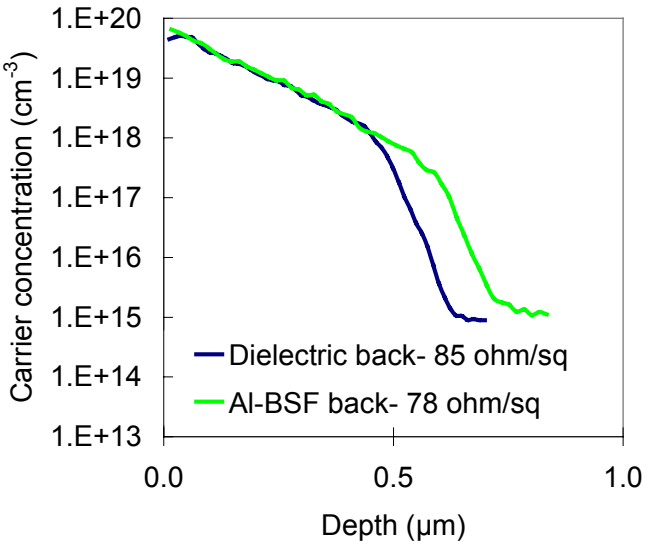


Figure 9.11 Emitter profiles used in the simulation of the dielectric and the Al-BSF back-passivated cells.

Table 9-4 Parameters used in the PC1D program to obtain the best fit of the IQE of the dielectric and the Al-BSF back-passivated cells.

Parameters		Dielectric		BSF back
		No light-bias	Light-bias	
BSRV (E_t=0, S_{n0}=S_{p0}) (cm/s)		20,000	125	300
FSRV (E_t=0, S_{n0}=S_{p0}) (cm/s)		16,000		18,500
SRH lifetime (E_t=0) τ_{n0}=τ_{p0} (μs)		1,200		500
Front internal reflection (specular) (%)	1st bounce	84		92
	Subsequent bounce	91		92
Back internal reflection (diffused) (%)	1st bounce	96		68
	Subsequent bounce	93		68
Front surface		Textured: angle 54.74°, depth 3.535 μm		
Substrate		300 μm, ρ=1.35 ohm-cm		

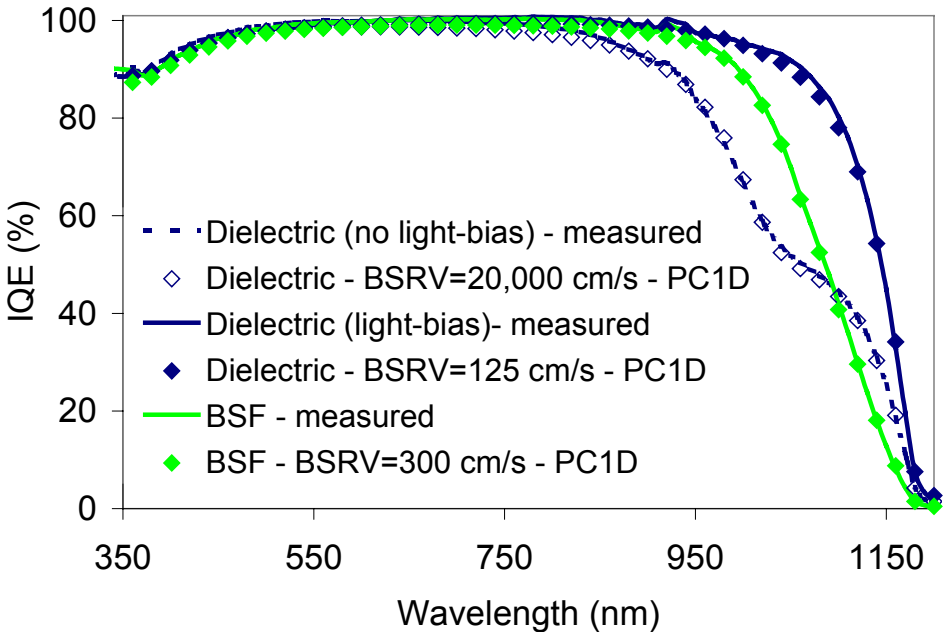


Figure 9.12 Comparison of the measured and the PC1D-simulated IQE curves of the dielectric and the Al-BSF back-passivated cells. The parameters used in the simulations are summarized in Table 9-4. Note that for the case of the dielectric back-passivated cell, the light-biased and no light-biased IQE curves were fitted separately by two different BSRV values.

From the fit to the front IQE, the FSRV values were found to be 16,000 cm/s and 18,500 cm/s for the dielectric and the Al-BSF back-passivated cells, respectively. The long wavelength IQE fitting gave a BSRV of 300 cm/s for the Al-BSF cell and a BSRV of 125 cm/s and 20,000 cm/s for the dielectric back-passivated cell with and without light bias, respectively.

In the next section, the extracted material and device parameters from the above sections were used to simulate the light I-V curves of the two cells. The explanation for the strong dependency of the IQE response with and without the light bias in the case of the dielectric back-passivated cell is also given in the next section.

9.3 Modeling of the Screen-Printed Dielectric Back-Passivated Solar Cell

In the previous section, important cell parameters were extracted through comprehensive characterizations of the dielectric back-passivated cell along with the conventional Al-BSF back-passivated reference cell. In this section, the extracted parameters were used to simulate the light I-V curves of the two cells. The simulated and the measured light I-V curves were then compared to validate the accuracy of the extracted cell parameters and to quantify the benefits of dielectric back passivation.

The simulation was first performed using the widely used PC1D program. The parameters extracted for the two cells (dielectric and full Al-BSF) were used as input parameters to generate the light I-V curves. As shown below, although the light I-V curve of the Al-BSF back-passivated cell could be replicated relatively well using the extracted parameters, there was a clear discrepancy between the simulated and the measured light I-V curves for the dielectric back-passivated cell. It will be shown later in this section that this discrepancy can be removed by either introducing a combination of the positive

charge density in the dielectric layer and the highly asymmetrical capture cross-section of holes and electrons at Si/SiO_2 interfaces or by introducing parasitic shunting of the inversion layer induced by the positive charge density in the rear dielectric. These effects can also account for the observed strong dependency of the long-wavelength IQE response to the light bias in Section 9.2.

After a good agreement between the simulated and the measured light I-V curves was obtained using the PC1D program, two-dimensional simulations by the Dessis program were performed to further investigate the effect of the LBSF in the dielectric back-passivated cell. Finally, additional simulations were performed to obtain a guideline for 20% efficient cells on thin Si substrates.

9.3.1 PC1D Simulation of the Dielectric and the Al-BSF Back-Passivated Cells

The light I-V curves of the dielectric and the Al-BSF back-passivated cells were generated using the PC1D program. The input parameters for the PC1D program are summarized in Table 9-5. Most of these parameters were from the analysis in the previous section.

Table 9-5 Input parameters used in the PC1D program to simulate light I-V curves of the dielectric and the Al-BSF back-passivated cells

Parameters		Dielectric back	BSF back	Acquiring method
BSRV (E_t=0, S_{n0}=S_{p0}) (cm/s)		125	300	Light-bias IQE fit
FSRV (E_t=0, S_{n0}=S_{p0}) (cm/s)		16,000	18,500	
SRH lifetime (E_t=0) τ_{n0}=τ_{p0} (μs)		1,200	500	Measured on adjacent wafers
Front internal reflection (specular) (%)	1st bounce	84	92	Escaped reflectance fit
	Subsequent bounce	91	92	
Back internal reflection (diffused) (%)	1st bounce	96	68	
	Subsequent bounce	93	68	
Series resistance (ohm-cm^2)		0.79	0.57	Light I-V measurement
Shunt resistance (ohm-cm^2)		35,540	84,000	
2nd diode	J_{02} (nA/cm^2)	142	397	Dark I-V fit
	n_2	2.24	2.55	
Front surface		Textured: angle 54.74°, depth 3.535 μm		Assumed
Front reflectance		From measured data with escaped reflectance removed and 4.65% absolute increased in reflection for all wavelength to account for gridlines shading		Measured reflectance+ calculated gridline shading from measured gridline width
Substrate		300 μm, ρ=1.35 ohm-cm		Measurement
Emitter profiles		Profile in Figure 9.11	Profile in Figure 9.11	Spreading resistance measurement

The measured and the simulated light I-V curves and parameters performance of the two cells are shown in Figure 9.13 and Table 9-6, respectively.

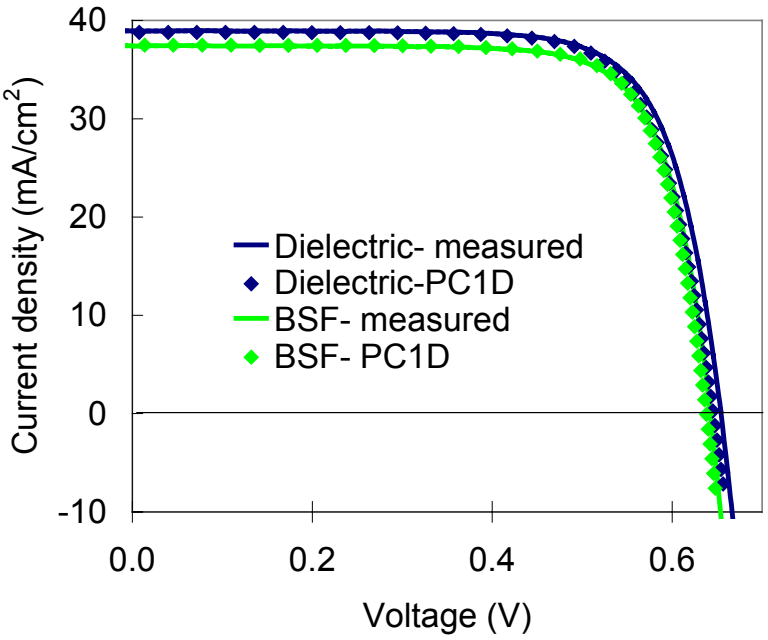


Figure 9.13 Comparison of the measured and the PC1D-simulated light I-V curves of the dielectric and the Al-BSF back-passivated cells. The parameters used in the simulations are summarized in Table 9-5.

Table 9-6 Comparison of the measured and the PC1D-simulated light I-V parameters of the dielectric and the Al-BSF back-passivated cells.

	Dielectric back		Al-BSF back	
	Measured	Simulated (fixed BSRV =125 cm/s)	Measured	Simulated (fixed BSRV =300 cm/s)
V_{oc} (mV)	654	646	643	638
J_{sc} (mA/cm^2)	38.9	38.8	37.4	37.5
FF (%)	74.8	75.2	76.0	77.0
Efficiency (%)	19.1	18.8	18.3	18.4

Figure 9.13 shows that, for the Al-BSF back-passivated cell, the PC1D-simulated I-V curve, using the input parameters in Table 9-5, matched the measured light I-V curve relatively well. This validates the methods used in the previous section to extract the input cell parameters. However, matching was not as good for the dielectric back-

passivated cell as the simulated I-V curve at low voltages matched quite well but started to deviate at higher voltages near V_{oc}. This result suggests that the fixed BSRV value of 125 cm/s used in the simulation, which was obtained by fitting the light-biased IQE (measured at short circuit condition), may not be valid at higher voltages. This finding in conjunction with the observed dependency of the long-wavelength IQE response on the light bias indicates that the BSRV of the dielectric back-passivated cell fabricated in this work is a strong function of the injection level and decreases with the increase in the injection level. This was studied by modeling in the next section.

9.3.2 Simulation of Dielectric Back-Passivated Cell to Explain the Voltage Dependency of the BSRV

The above behavior of the dielectric back-passivated cell can be caused by either (1) the combined effect of the positive charge density in the dielectric layer and a highly asymmetrical capture cross section of electrons and holes at the Si/SiO_2 interface states or (2) the effect of shunting of the inversion layer induced by the positive charge density in the dielectric layer. In this section, these two effects were simulated to explain this behavior and to enhance the accuracy of simulating the dielectric back-passivated cell. The first scenario was simulated by introducing a positive charge density and specific S_{n0} and S_{p0} values at the back surface. In the second scenario, in addition to the positive charge density and the specific S_{n0} and S_{p0} values, a shunt path between the inversion layer and the back contact were introduced. Either a resistor or a diode can be used to represent the shunt path. Thus, three models of the back surface were incorporated in the simulations (Figure 9.14). For all three cases, the S_{n0} and S_{p0} values were fixed at 1,000 cm/s and 15 cm/s, respectively. These values were taken from [127] where they were used to explain the recombination activity at Si/SiO_2 interfaces.

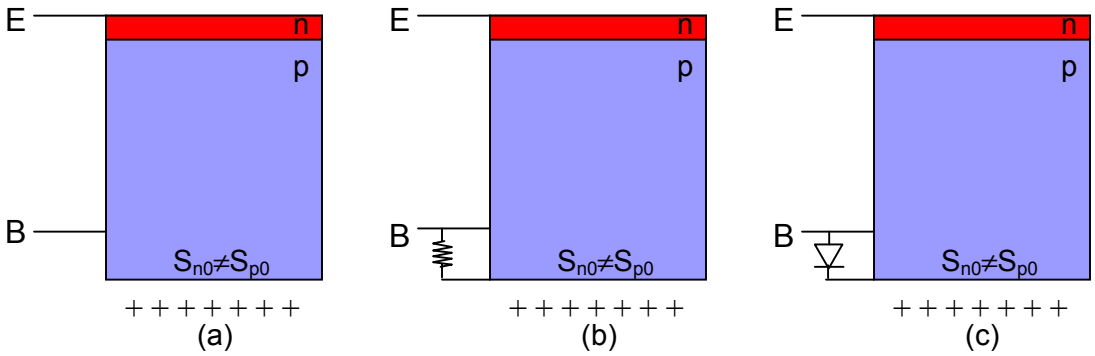


Figure 9.14 Schematic representation of the three back models applied in the PC1D program to improve the simulation of the dielectric back-passivated cell: (a) introduction of fixed positive charge and asymmetrical S_{n0} and S_{p0} on the back surface, (b) same as (a) but with a resistive shunt path between the inversion layer and the base contact, and (c) same as (a) but with a rectifier shunt path between the inversion layer and the base contact. E and B represent emitter and base contacts, respectively. In all cases, S_{n0} and S_{p0} were fixed at 1,000 cm/s and 15 cm/s, respectively.

Each of these three cases shown in Figure 9.14 contained at least one new parameter that required a value assignment. In Case (a), the positive charge density needed to be assigned. In Case (b), the positive charge density and the resistance of the parasitic shunt resistor needed to be assigned. In Case (c), the positive charge density and the J_0 and the n values of the parasitic shunt rectifier needed to be assigned. The methods and assumptions used in assigning the values of these parameters are explained below.

For all three models, the common strategy used in assigning the parameter values was to match the J_{sc} value of 38.8 mA/cm^2, which corresponds to a BSRV value of 125 cm/s (Table 9-6). The simulation to match the J_{sc} value was performed in the PC1D program using the exact same parameters shown in Table 9-5 but instead of fixing the BSRV value, each of the three back models in Figure 9.14 was applied.

The positive charge density in Case (a) was assigned by varying the positive charge density from 1.1×10^{11} to 2.2×10^{11} cm^{-2} to obtain the J_{sc} value of 38.8 mA/cm^2. This range of the positive charge density was selected based on the measured charge density in the

spin-on SiO_2/LF-SiN_x layer by the surface charge analyzer (as reported in Chapter 8). The calculated values of J_{sc} and V_{oc} for this back surface model as a function of the positive charge density are shown in Table 9-7. The simulations reveal that the V_{oc} is not a strong function of the positive charge density in the range of interest, while the J_{sc} is. The charge density of 1.12×10^{11} cm^{-2} was found to give the best match of the J_{sc} value of 38.8 mA/cm^2.

For back surface models (b) and (c), the positive charge density was fixed at 2.2×10^{11} cm^{-2}, which, according to PC1D, is the onset of shunting for 1.35 ohm-cm p-type cells with the current design. The charge density of 2.2×10^{11} cm^{-2} is also within the range of the charge density measured in the spin-on SiO_2/LF-SiN_x with the surface charge analyzer.

In Case (b), the resistance of the back resistive shunt path in the PC1D program was varied to obtain the J_{sc} value of 38.8 mA/cm^2. Similar to Case (a), only the J_{sc} was found to be a strong function of the resistance values investigated. The resistance value of 1,590 ohm was found to give the best match to the J_{sc} value of 38.8 mA/cm^2.

In Case (c), for simplicity, the diode ideality factor was first fixed to 3.0. The J_0 value of the parasitic shunt rectifier was then varied to obtain the J_{sc} value of 38.8 mA/cm^2. Similar to Cases (a) and (b), J_{sc} was found to be a strong function of J_0 of the shunting diode while V_{oc} was relatively independent of the J_0 values investigated. The J_0 value of 255 nA for this back surface model was found to give the best match to the J_{sc} value of 38.8 mA/cm^2.

Note that by incorporating each of the three back surface models, the V_{oc} became more consistent with the measured V_{oc} of 654 mV (Cell D-5 in Table 9-1).

Table 9-7 J_{sc} and V_{oc} as a function of the positive charge density in the dielectric layer using Structure (a) in Figure 9.14.

Charge (cm^{-2})	1.10×10^{11}	**1.12×10^{11}**	1.25×10^{11}	1.50×10^{11}	2.20×10^{11}
J_{sc} (mA/cm^2)	38.5	**38.8**	39.0	39.1	39.1
V_{oc} (mV)	653	**653**	654	654	654

Table 9-8 J_{sc} and V_{oc} as a function of the resistance of the back resistive shunt path using Structure (b) in Figure 9.14. The positive charge density was fixed at 2.2×10^{11} cm^{-2}.

Shunt resistance (Ω)	1,000	**1,587**	2,500	10,000	∞
J_{sc} (mA/cm^2)	38.6	**38.8**	38.9	39.1	39.1
V_{oc} (mV)	654	**654**	654	654	654

Table 9-9 J_{sc} and V_{oc} as a function of J_0 of the back rectifier shunt path using Structure (c) in Figure 9.14. The positive charge density was fixed at 2.2×10^{11} cm^{-2} and n was fixed at 3.

J_0 (nA)	400	**255**	200	100	0
J_{sc} (mA/cm^2)	38.6	**38.8**	38.9	39.0	39.1
V_{oc} (mV)	653	**653**	653	654	654

After matching the V_{oc} and the J_{sc}, each of the three back surface models was used to simulate the long-wavelength IQE response without the light bias. The measured and simulated IQE for the three models are plotted in Figure 9.15. All three models were able to match the measured IQE response without light-bias quite well. However, it should be noted that the simulated long-wavelength IQE responses for all three models were found to be strong functions of the light intensity used in the PC1D program. Therefore, the light intensity was adjusted in the PC1D program to obtain the best fit to the IQE. A lower intensity of 1×10^{-4} W/cm^2 was required to obtain the best fit in the case of the rectifier shunt path model as opposed to an intensity of 8×10^{-4} W/cm^2 for the charge-only and the resistive shunt path models.

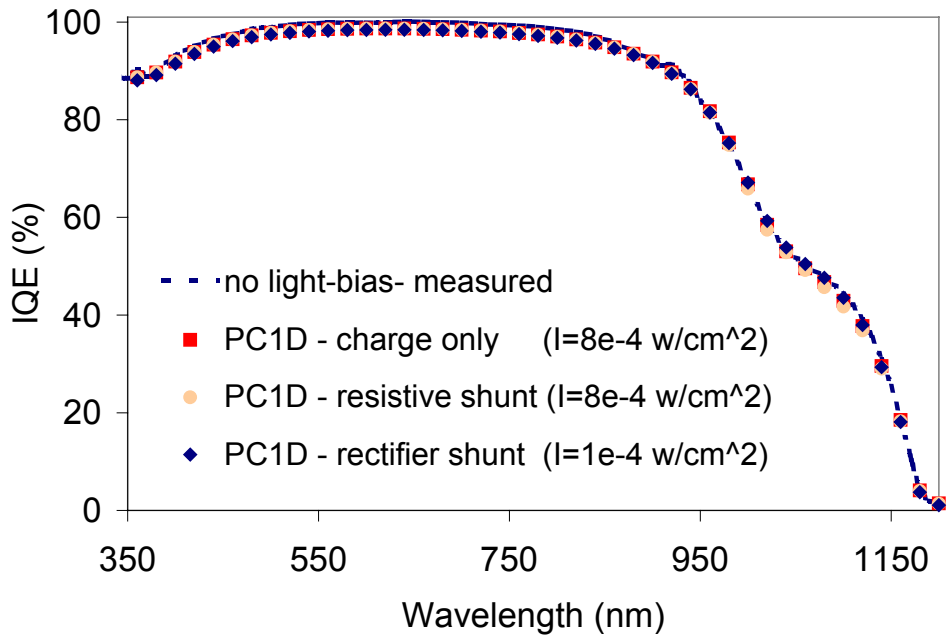
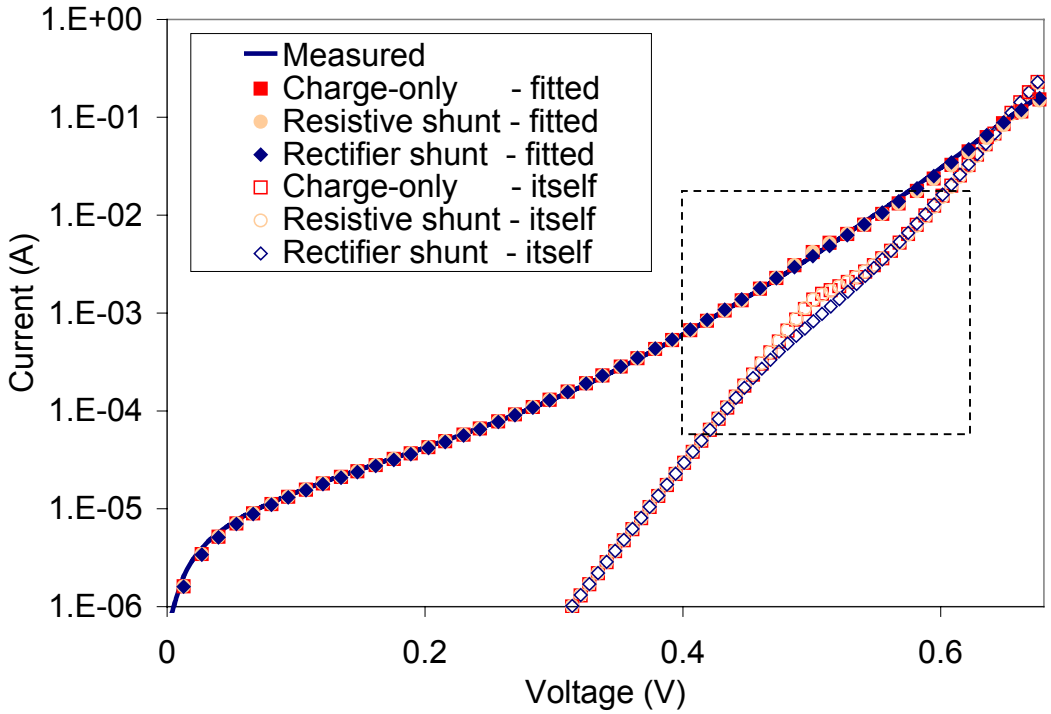


Figure 9.15 Comparison of the measured and the PC1D-simulated IQE of the dielectric back-passivated cell with improved back surface models (Figure 9.14). Note that for the case of a rectifier shunt path, the intensity of the incident light used to obtain the best fit was 1×10^{-4} W/cm^2 as opposed to 8×10^{-4} W/cm^2 for the cases of charge-only and a resistive shunt path.

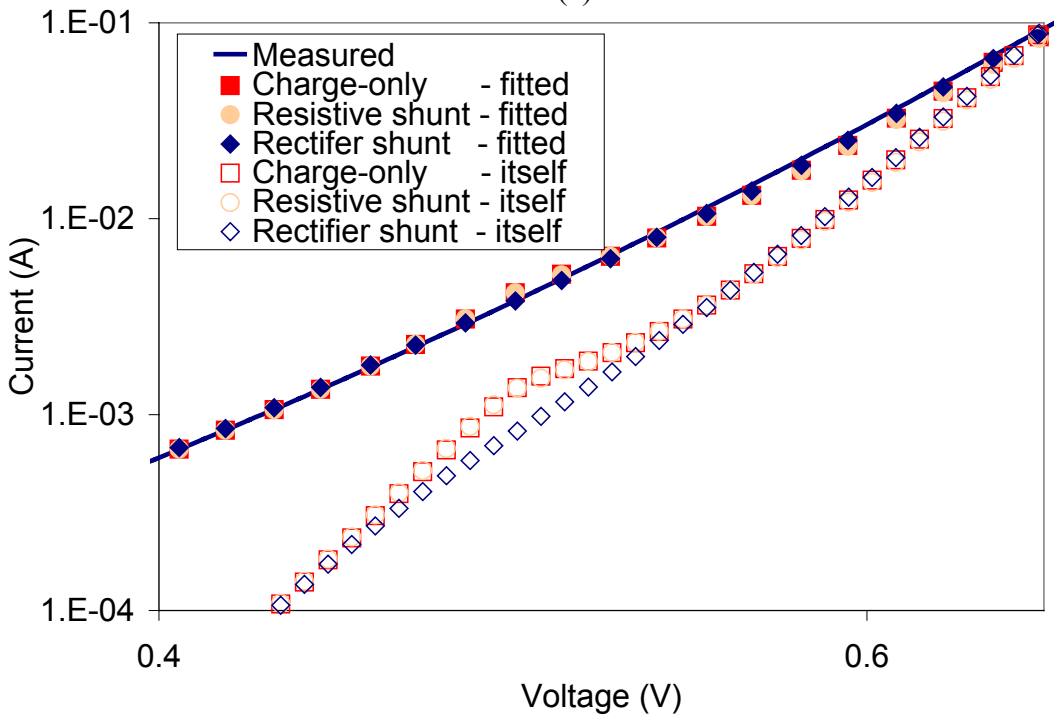
Since the introduction of the new back surface model may also affect the dark I-V curve, it was instructive to refit the measured dark I-V curve using each of the above back surface models. This was done by first simulating the relationship between I_{d1} and V_{d1} (in Figure 9.5) in the PC1D program using each back surface model. Best fit between the measured and the simulated dark I-V was then obtained varying the J_{02} and n_2 values with fixed R_{sh} to the measured value in Table 9-1 and fixed R_s to the calculated value using Equation 9.3 (the same method used in Section 9.2.2). The values of J_{02} and n_2 that gave the best fit for each of the three back surface models are summarized in Table 9-10, and Figure 9.16 shows the corresponding fit.

Table 9-10 Extracted J_{02} and n_2 from dark I-V fitting for each of the three back models in Figure 9.14.

Configuration	J_{02} (nA/cm^2)	n_2
Charge-only	179	2.35
Resistive shunt	179	2.36
Rectifier shunt	159	2.31



(a)



(b)

Figure 9.16 Measured and simulated dark I-V curve for each of the three back models: (a) the overall dark I-V curves and (b) the magnified view at ~0.5 V to show the kink in the charge-only and resistive shunt path models. Also included in the figures are the dark I-V curves for the three models prior to the fitting (i.e., the dark I-V curves without R_s, R_{sh}, and 2nd diode effects).

As shown in Figure 9.16a, the overall dark I-V curve could be fitted relatively well using any of the three back surface models. To establish which of the models is most applicable to the current device, the dark I-V curve for each of the three back surface models without the R_s, R_{sh}, and J_{02} components was calculated and is included in Figure 9.15 (denoted "- itself"). The calculations show that the first two back surface models exhibit a kink at ~0.5 V, but the third model, which involving rectifier shunt, does not. A magnified view of the kink area in Figure 9.15b revealed that the kink could also be observed in the fitted dark I-V curves by the first two back surface models. Since experimental data exhibited no kink, it suggests that the dielectric back-passivated cell in this study could be best described by the shunting of the inversion layer that is described by a rectifier shunt path.

Finally, the light I-V curves were generated using the three back surface models with their corresponding J_{02} and n_2 in Table 9-10. Except for the BSRV, the J_{02}, and the n_2 values, all the other input parameters were kept the same as in Table 9-5. The simulated light I-V curves for the three models are plotted in conjunction with the measured light I-V curve in Figure 9.17. The previously simulated light I-V curve using a fixed BSRV value of 125 cm/s was also included in the figure for comparison. The measured and the simulated light I-V parameters are summarized in Table 9-11.

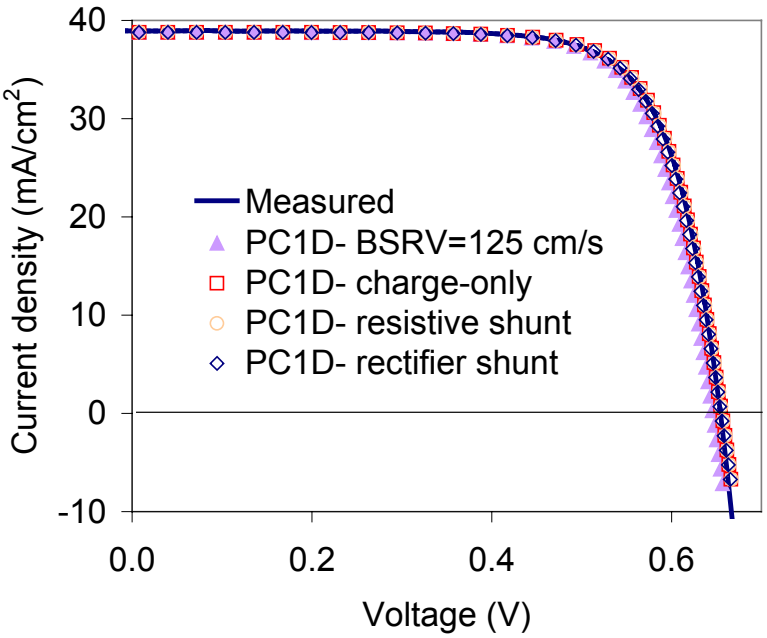


Figure 9.17 Comparison of the measured and the PC1D-simulated light I-V curves of the dielectric back-passivated cell for different back surface configurations: (a) fixed BSRV of 125 cm/s, (b) charge-only model, (c) resistive shunt model, and (d) rectifier shunt model.

Table 9-11 Comparison of the measured and the PC1D-simulated light I-V parameters of the dielectric back-passivated cell.

	Measured	PC1D-simulated			
		125 cm/s	Charge-only model	Resistive shunt model	Rectifier shunt model
V_{oc} (mV)	654	646	656	656	655
J_{sc} (mA/cm^2)	38.9	38.8	38.8	38.8	38.8
FF (%)	74.8	75.2	75.5	75.5	75.2
Efficiency (%)	19.1	18.8	19.2	19.2	19.1

As can be seen from Figure 9.17 and Table 9-11, the matching between the simulated and the measured I-V curves of the dielectric back-passivated cell was improved significantly by introducing each of the three back surface models. This is because the

BSRV becomes a function of the injection level in the three back surface models. This showed the importance of charge, asymmetric S_{n0} and S_{p0}, and parasitic shunting in dictating the behavior of the dielectric back-passivated cell. It should be noted that even though the effect of the LBSF could not be included in the 1-D program, the light I-V curve could already be matched quite well using the PC1D program. Nevertheless, 2-D simulations were performed using the Dessis simulation program to confirm the validity of the 1-D simulation, which excludes the effect of the LBSF.

9.3.3 Two Dimensional Device Simulation Using Dessis to Explain the Difference in the Dielectric and the Al-BSF Back-Passivated Cells

The Dessis simulation was performed to account for the multi dimensional nature of the dielectric back-passivated cell. Although, the actual back contact design of a point contact geometry used in the actual cell would require a 3-D simulation, a 2-D simulation was employed to avoid excessive computational time. Here, the 2% area fraction of the metal on the back surface (125-μm diameter (resulted from the paste spreading from a 100-μm on-screen design) and 800-μm center-to-center spacing) was modeled. The unit cell used to simulate the dielectric back-passivated cell in the Dessis program is shown in Figure 9.18. Note that the back contact in this simulation was designed such that (1) there is negligible impact from the recombination at the edge of the back contact (i.e., a BSF region was introduced to completely isolate the metal back contact) and (2) there is a separate back contact located next to the dielectric layer, which acts as a parasitic shunt path to the inversion layer. The width of the parasitic shunt contact was made very small (2 nm) to ensure that there is a minimal impact of the recombination at the parasitic shunt contact itself. The work function of the back contact and the parasitic shunt contact was set to 4.1 eV to ensure complete shunting to the inversion layer, as discussed in Chapter

7. The combination of a BSF layer with a doping concentration of 3×10^{18} cm^{-3} and a thickness of 3.4 μm and a heavily doped layer with a doping concentration of 1×10^{21} cm^{-3} and a thickness of 20 nm (introduced to activate a tunneling contact as explained in Chapter 7) gave an effective surface recombination velocity of 300 cm/s on a 1.35 ohm-cm p-type substrate (verified by the PC1D program). In other words, the recombination velocity at the LBSF of the dielectric back-passivated cell was assumed to be 300 cm/s, which is the BSRV value that was extracted from the full-area Al-BSF back-passivated cell in the previous section.

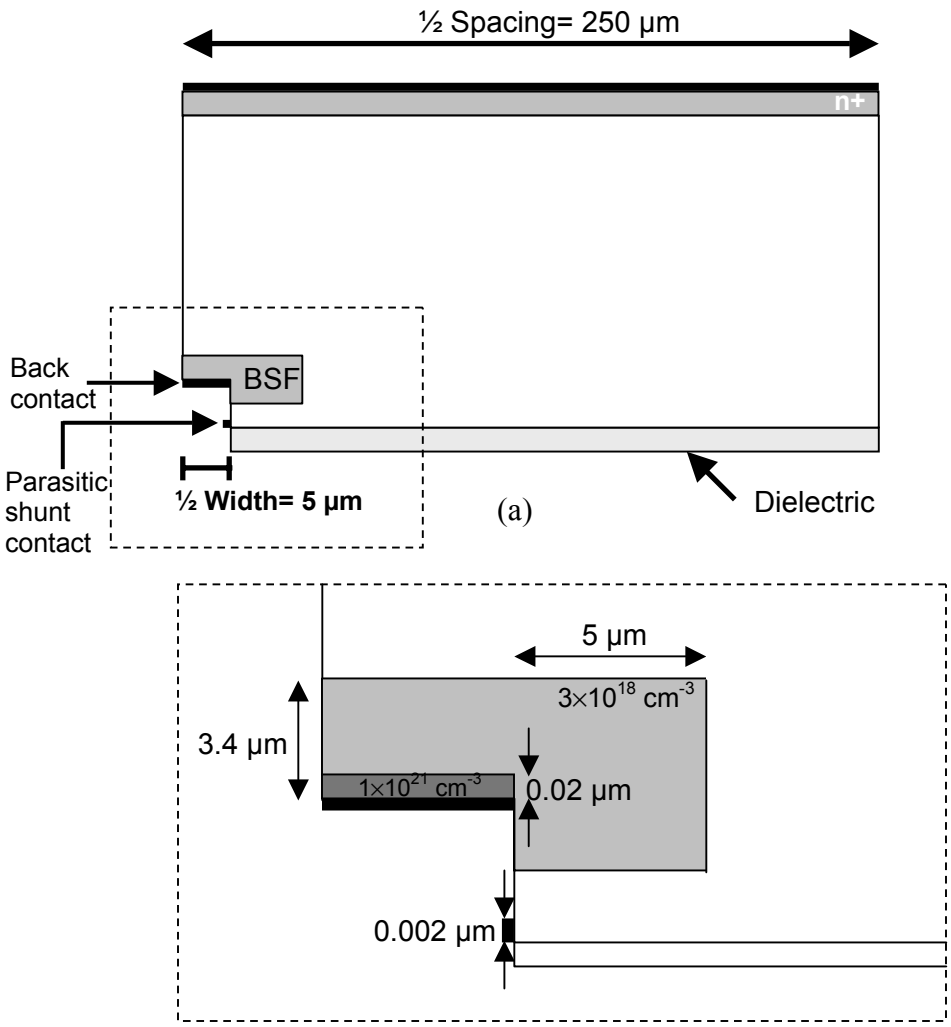


Figure 9.18 Simulation domain used in the Dessis program to simulate the dielectric back-passivated cell: (a) the overall structure and (b) the magnified view at the back contact. Two main features included are (1) a wrapped-around BSF to minimize the impact of the recombination at the edge of the back contact and (2) a small contact located next to the dielectric layer to act as a parasitic shunt path to the inversion layer induced by charge in the dielectric.

Furthermore, to replicate the PC1D simulation by the Dessis program, the following steps were taken:

(a) Ensure that the same physical models and parameters were used in the Dessis program.

The primary models included in the Dessis program are

(1) *Temperature=298.15*,

(2) *EffectiveIntrinsicDensity(delAlamo)*: using the same parameters used in the PC1D program,

(3) *Mobility (PhuMob (Phosphorus))*: using the default parameters given in the Dessis version 10,

(4) *Recombination (SRH Auger)*: using the same Auger coefficients used in the PC1D program,

(5) *OpticalGeneration* using the AM1.5G data from the PC1D program

(6) *Recombination (BarrierTunneling)*, activated for the back and the parasitic shunt contacts: using the default parameters given in the Dessis version 8.

(b) Reduce the bulk lifetime to account for the band-to-band recombination, which was activated in the PC1D program but not in the Dessis program.

(c) Adjust the internal front and back surface reflection in the Dessis program to match the cumulative optical generation from the PC1D program.

(d) Enhance FSRV and area factor in the Dessis program to account for the electrical effects of textured surfaces that was included in the PC1D program. To obtain the corresponding FSRV and area factor values for the Dessis program, the following

steps were taken: (1) simulate the dielectric back-passivated cell (with a rectifier shunt path) using the PC1D program with the "front surface textured" feature activated, (2) turn-off the "front surface textured" feature, (3) increase the FSRV to obtain the same V_{oc} as obtained when the "front surface textured" feature was activated, and (4) increase the cell area to obtain the same J_{sc} as obtained when the "front surface textured" feature was activated. Following the above procedure, the FSRV of 38,500 cm/s (in place of 16,000 cm/s) and the area of 1.008 cm^2 (in place of 1 cm^2) were obtained.

To replicate the behavior of the shunt path, the same way it was applied in the PC1D program, a rectifier shunt diode with J_0 of 255 nA and n of 3.0 was introduced between the back contact and the parasitic shunt contact as shown in Figure 9.19. Note that, for simplicity, the Dessis program was used only for the simulation of the primary diode and the parasitic shunt diode: other resistance and leakage components, i.e., R_s, R_{sh} and 2nd diode, were calculated outside the Dessis program using circuit equations.

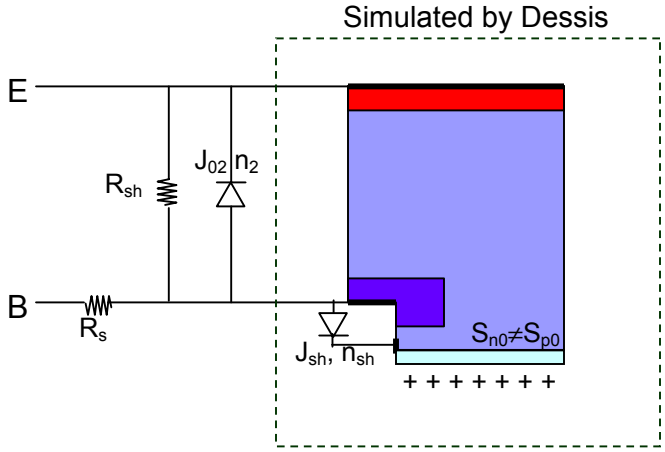


Figure 9.19 Schematic representation of the circuit used in simulating the dielectric back-passivated cell with the Dessis program. Note that only the cell itself and the parasitic shunt diode were simulated using the Dessis program.

To ensure that the simulation results from the Dessis program were consistent with the PC1D program, the light I-V curve of the Al-BSF back-passivated cell was also simulated using the Dessis program. All parameters used in simulating the dielectric and the Al-BSF back-passivated cells in the Dessis program are summarized in Table 9-12. The Dessis-simulated light I-V curves along with the measured light I-V curves for both the cells are plotted in Figure 9.20. Additionally, the measured and the Dessis-simulated light I-V parameters of both the cells are summarized in Table 9-13.

Table 9-12 Input parameters for the Dessis program to simulate light I-V curves of the dielectric and the Al-BSF back-passivated cells

Parameters		Dielectric back	BSF back	Acquiring method
BSRV at the back dielectric (E_t=0) (cm/s)	S_{n0}	1,000	-	From literature
	S_{p0}	15	-	
Charge in the back dielectric (cm^{-2})		2.2×10^{11}	-	PC1D analysis in Section 9.3.2
Effective SRV at the back contact (cm/s) (by an introduction of a BSF)		300	300	- IQE fit of the BSF cell - Assumed the same for the LBSF of the dielectric back cell
FSRV (cm/s)		35,800	42,500	Enhanced FSRV by matching V_{oc} of cells with textured and planar surfaces in PC1D
SRH lifetime (E_t=0) $\tau_{n0}=\tau_{p0}$ (μs)		1,100	475	Measured
Optical generation	Front internal reflection (%)	81.6	70.0	To match cumulative optical generation from PC1D
	Back internal reflection (%)	90.0	68.0	
	Intensity spectrum	From PC1D AM1.5G de-rated by 4.65% to account for gridline shading		Calculated gridline shading from measured gridline width
	Anti-reflection	n=2.0, thickness=750 Å		Assumed
	Surface angle (°)	54.74		Assumed
Area factor (%)		100.8		Enhanced area factor by matching J_{sc} of cells with textured and planar surfaces in PC1D
Series resistance ($ohm\text{-}cm^2$)		0.79	0.57	Light I-V
Shunt resistance ($ohm\text{-}cm^2$)		35,540	84,000	
2^{nd} diode	J_{02} (nA/cm^2)	159	397	Dark I-V fit
	n_2	2.31	2.55	
Parasitic shunt diode	J_0 (nA)	255	-	PC1D analysis in Section 9.3.2
	n	3.00	-	
Substrate		300 μm, ρ=1.35 ohm-cm		Measured
Emitter profiles		Profile in Figure 9.11	Profile in Figure 9.11	Spreading resistance measurement

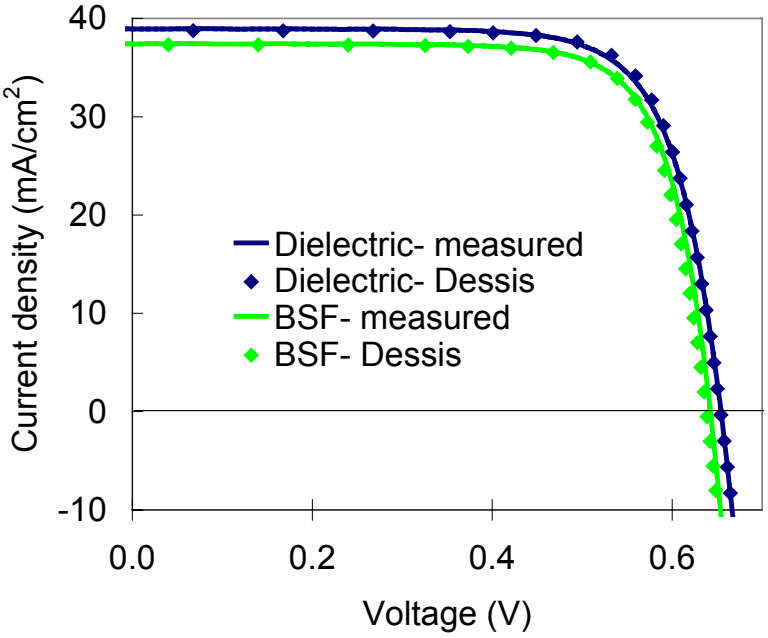


Figure 9.20 Comparison of the measured and the Dessis-simulated light I-V curves of the dielectric and the Al-BSF back-passivated cells. The parameters used in the simulations are summarized in Table 9-12.

Table 9-13 Comparison of the measured and the Dessis-simulated light I-V parameters of the dielectric and the Al-BSF back-passivated cells.

	Dielectric back		Al-BSF back	
	Measured	Simulated	Measured	Simulated
V_{oc} (mV)	654	654	643	638
J_{sc} (mA/cm^2)	38.9	38.8	37.4	37.3
FF (%)	74.8	75.2	76.0	76.9
Efficiency (%)	19.1	19.1	18.3	18.3

As can be seen in Figure 9.20, the Dessis simulations replicated the light I-V curves of both the cells quite well. The fact that the light I-V curve of the Al-BSF back-passivated cell could be fitted reasonably well validated the consistency between the Dessis and the PC1D programs for a 1-D device. On the other hand, the fact that the

dielectric back-passivated cell could be fitted quite well using either the PC1D program or the Dessis program, which includes the LBSF effect, suggests that the LBSF with an effective BSRV of 300 cm/s has minimal impact on cell performance of the current cell structure.

In the next section, the PC1D program was then used to establish a guideline for 20% efficient cells on thin Si substrates based on the dielectric back-passivated cell developed in this work.

9.3.4 Guideline for 20% Efficient Cells on Thin Si Substrates

Based on the analysis of the dielectric back-passivated cell in the previous sections, guidelines for achieving 20% efficient cells were established in this section. The dielectric back-passivated cell with the rectifier parasitic shunt path introduced in section 9.3.2 was used to generate guidelines summarized in Figure 9.21, where the solar cell efficiency is plotted as a function of the thickness of the substrate. The two highlighted data points in the figure correspond to the 19% dielectric back-passivated screen-printed cell achieved in this study on a 300-μm thick Si substrate and the target value of 20% dielectric back-passivated cells on a 100-μm thick Si substrate.

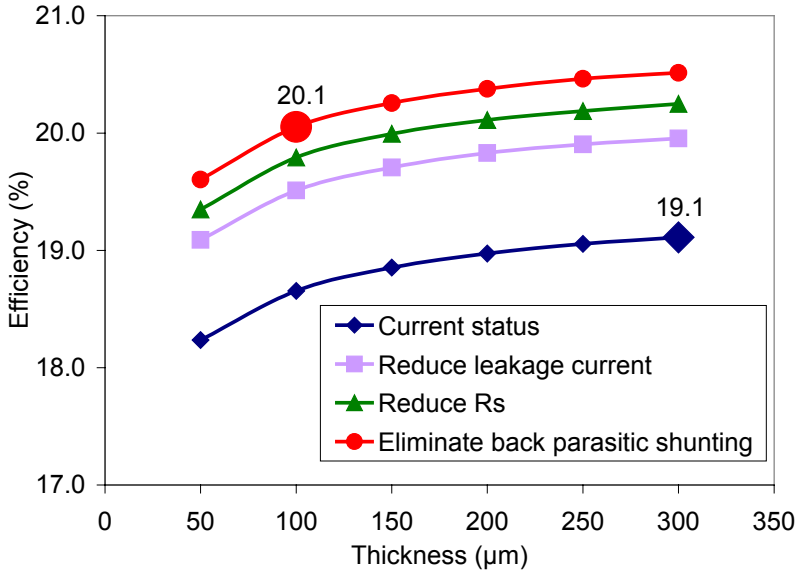


Figure 9.21 Guidelines for 20% efficient solar cells on thin Si substrates. The two highlighted points in the figure indicate current status of a 19% dielectric back-passivated cell with a 300-μm thick Si substrate and the target status of a 20% dielectric back-passivated cell with a 100-μm thick Si substrate.

As shown in Figure 9.21, three improvements are required to achieve the target value of 20% efficient in 100-μm thick cells:

(a) Reduction of the leakage current: reduce the J_{02} from 159 nA/cm^2 (with n_2=2.3) to 18.5 nA/cm^2 (with n_2=2.1)

(b) Reduction of the R_s value from 0.79 ohm-cm^2 to 0.57 ohm-cm^2

(c) Elimination of the back parasitic shunt path (between the inversion layer and the back contact)

As can be seen in the figure, the reduction in the leakage current (J_{02}) has the highest impact on the efficiency (about 0.8% absolute improvement in the efficiency). The J_{02} value of 18.5 nA/cm^2 with n_2=2.1 was chosen, as these values have been demonstrated in [134] using a screen-printed contact on a high sheet resistance emitter. The reduction of R_s to 0.57 ohm-cm^2 gave another 0.2-0.3 % absolute improvement in the efficiency. This value was chosen, because it was achieved in this work on the Al-BSF back-passivated

cell (but not on the dielectric back-passivated cell). Finally, based on the hypothesis of the cell being affected by a rectifier shunt path on the back, the elimination of this shunt path can further improve the cell efficiency by another 0.3% absolute.

9.4 Conclusions

Through the implementation of the metallization technique and the dielectric layer developed in this thesis, a screen-printed dielectric back-passivated Si solar cell was fabricated that achieved as high efficiency as 19% on a 300-μm thick FZ Si substrate. This dielectric back-passivated Si solar cell produced about 0.3-0.8% absolute efficiency higher than that of the conventional Al-BSF back-passivated Si solar cell with a similar front structure.

Through detailed characterizations and analyses, the dielectric back-passivated cell fabricated in this work was simulated with high accuracy using the 1-D simulation PC1D program, as well as the 2-D simulation program Dessis. A good match was obtained between the measured and simulated cells. The analysis revealed that to achieve 20% efficient 100-μm thick cells for grid parity, three main areas of development are required: (1) reduction of the leakage current (J_{02}) from 159 nA/cm^2 (with n_2=2.3) to 18.5 nA/cm^2 (with n_2=2.1), (2) reduction of the R_s from 0.79 ohm-cm^2 to 0.57 ohm-cm^2, and (3) elimination of the back parasitic shunt path because of the rear inversion layer.

CHAPTER 10

GUIDELINES FOR FUTURE WORK

A simple process scheme to fabricate high-efficiency dielectric back-passivated screen-printed p-type Si solar cells was developed in this thesis that features only one high temperature furnace step and full compatibility with screen-printing technology. The dielectric back-passivated screen-printed cell fabricated with this process achieved efficiency as high as 19.1% compared to 18.3% for a conventional full-area Al-BSF back-passivated cell with a similar front structure. However, there are several aspects of the cell characteristics and the fabrication process that can further be improved for higher efficiency and manufacturability. This chapter provides guidelines for future research and development topics to produce high-efficiency commercially viable dielectric back-passivated screen-printed solar cells.

Four main areas of future development are outlined below: (1) use of large-area and low-cost Si substrates, (2) higher quality contact formation, (3) higher throughput process to form SiO_2 for back surface passivation, and (4) use of modified Al-paste for industrial compatibility.

10.1 Large-Area and Low-Cost Substrates

Three changes are suggested in the area of the Si substrate. First, a larger substrate should be used. A typical size of single crystalline solar cells in industry today is five inches or six inches pseudo square. Consequently, there is a need to make 149 or 236 mm^2 dielectric back-passivated cells using the technology and dielectric developed to make 4 cm^2 cells in this work. Technology transfer to a larger area cell may require

modifications to the processing parameters and the equipments. The second aspect requires investigation of the use of Cz Si in place of FZ Si to lower the substrate cost. To avoid the LID effect, Ga-doped Cz, low-O_i MCz Si, or higher resistivity (≥ 3 ohm-cm) Cz should be used instead of regular 1-3 ohm-cm B-doped Cz Si. The third aspect calls for using thinner Si substrates to take advantage of the electrical and optical confinement of the dielectric back-passivated cells. This is the main motivation for the development of the dielectric back passivation in place of the conventional Al-BSF passivation because it will reduce the cell cost dramatically without sacrificing the cell efficiency and eliminate warpage.

10.2 High-Quality Contact Formation

It is clear from the cell analysis in Chapter 9 that there is considerable room for improvement in the FF of the dielectric back-passivated cell developed in this work. The analysis revealed that the emphasis should be placed first on the reduction of the junction leakage current followed by the reduction in the series resistance. These can be achieved through an improved front-contact formation. It may require a combination of emitter profile optimization, Ag-paste modification, and contact firing optimization.

Back contact formation should also be improved because the analysis revealed that the cell performance is also limited by parasitic shunting between the back contact and the inversion layer induced by the positive charge in the dielectric layer. Two possible sources of shunting are illustrated in Figure 10.1: (1) shunting of the dielectric inversion layer by the Al metal at the edge of the local opening and (2) shunting of the dielectric inversion layer by the Al metal via pinholes in the dielectric layer. The first source can be eliminated or alleviated by improving the edge definition of the opening so that the LBSF

can be formed uniformly at the edge of the contact. For the latter source, it is expected that improving the uniformity of the SiN_x deposition can help in eliminating the pinholes. Alternatively, it is also expected that the use of a dielectric layer with a lower positive charge density could also eliminate the shunting issue.

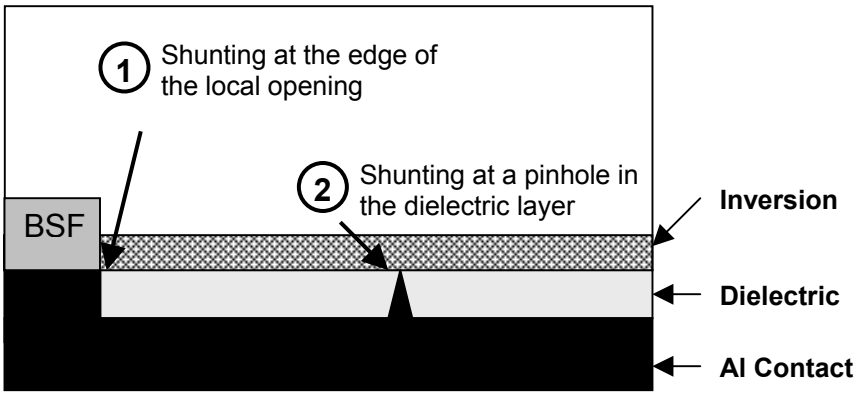


Figure 10.1 Two possible shunt paths between the back dielectric-induced inversion layer and the back contact: (1) at the edge of the local opening and (2) at a pinhole in the dielectric layer.

10.3 Development of a High-Throughput Process to Form the Back SiO_2 Layer

The back SiO_2 layer was formed in this work by the spin-on technology, which is not entirely compatible with high-throughput process and also requires excess use of a precursor. The spray-on technology, used in industry for dopants, could be a great alternative to overcome this limitation.

10.4 Modification of the Al-Paste to Improve Industrial Compatibility

The Al paste with Si content used in this work was found to form beads on the external surface of Al after annealing. Even though these beads can be easily removed by rubbing against the surface, it introduces an additional and unnecessary process step and

increases the probability of wafer breakage. A modification to the paste composition may be required to overcome this issue.

Another area of Al-paste development is to improve adhesion of the Al layer after annealing. This can also be realized through a modification of the paste composition.

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